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Switched-compensation technique in switched-capacitor circuits for achieving fast settling performance

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Switched-compensation technique in switched-capacitor circuits for achieving fast settling performance

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DEDICATION

To my parents

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ABSTRACT

Resolving stability issue is one of the major challenges in designing a perfect op-amp, the most widely used analog circuit block. Many compensation techniques have been proposed to improve the stability performance of op amps, but virtually all these techniques were developed for continuous-time applications and subsequently applied to discrete-time applications (e.g., switched-capacitor circuits). Since the early 1980s, an increasing number of op-amps have been used in switched-capacitor circuits with no special compensation method applied. Consequently, there remains a need to explore the possibility of designing a unique compensation method specifically for switched-capacitor use.

A new switched-compensation technique (SCT) is proposed for switched-capacitor circuit applications in which high speed is a critical index of performance. In general, designers must deal with trade-offs among accuracy, speed, and power dissipation. SCT avoids traditional approaches of designing high-speed, high-gain operational amplifiers that are in many cases technology-limited. Instead, it modifies the switched-capacitor circuit structure to use the under-damped response of the system, usually regarded as a drawback. SCT is introduced as a novel solution for achieving fast settling performance and lower quiescent power dissipation while guaranteeing almost equivalent accuracy. SCT can be easily implemented in flip-around switched-capacitor amplifier circuits. This paper explains SCT principle and implementation applied to multiplying-digital-to-analog converters (MDACs) as a proof of concept. Simulation results based on an IBM 0.13 μm CMOS process are presented. Compared with a conventional switched-capacitor amplifier, a SCT-based implementation reduces the quiescent power consumption by half and settling time within 1% error by 60%.

CHAPTER 1. INTRODUCTION

1.1 Motivation

The trend in current semiconductor technology is to continue scaling down the minimum transistor channel length. Figure 1.1 [1] illustrates the contemporary trend in transistor-size scaling by mainstream companies. Significant change in transistor feature size occurs every two or three years especially in the complementary metal-oxide-semiconductor (CMOS) process.

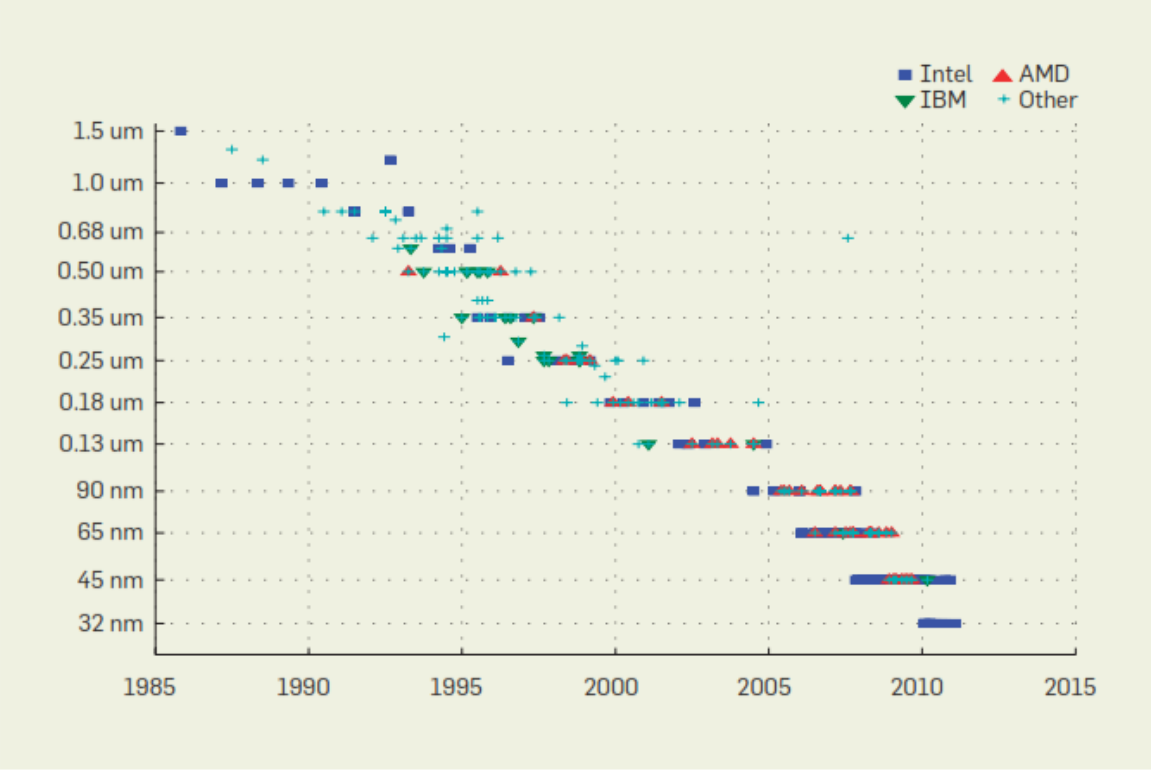


Figure 1.1: Scaling of transistor feature size over time

Such feature-size reduction produces higher chip integration density resulting in reduction in manufacturing cost of any particular functional circuit. To illustrate potential speed im-

provement, the expression for a short channel MOSFET transition frequency f_T is given as 1.1.

$$f_t \propto V_{EB}/L_{eff} \tag{1.1}$$

It is clear that a shorter channel-length transistor should enable high-speed design. Although this expectation may provide circuit designers with greater freedom in high speed circuit design, many challenges remain due to the physical limitations such as heat dissipation, charge leakage, noise, jitter, and process variation. For these reasons, the operating frequency of many circuits, especially CPUs, have not increased since 2005. Figure 1.2 [1] shows the processor frequency scaling with respect to time.

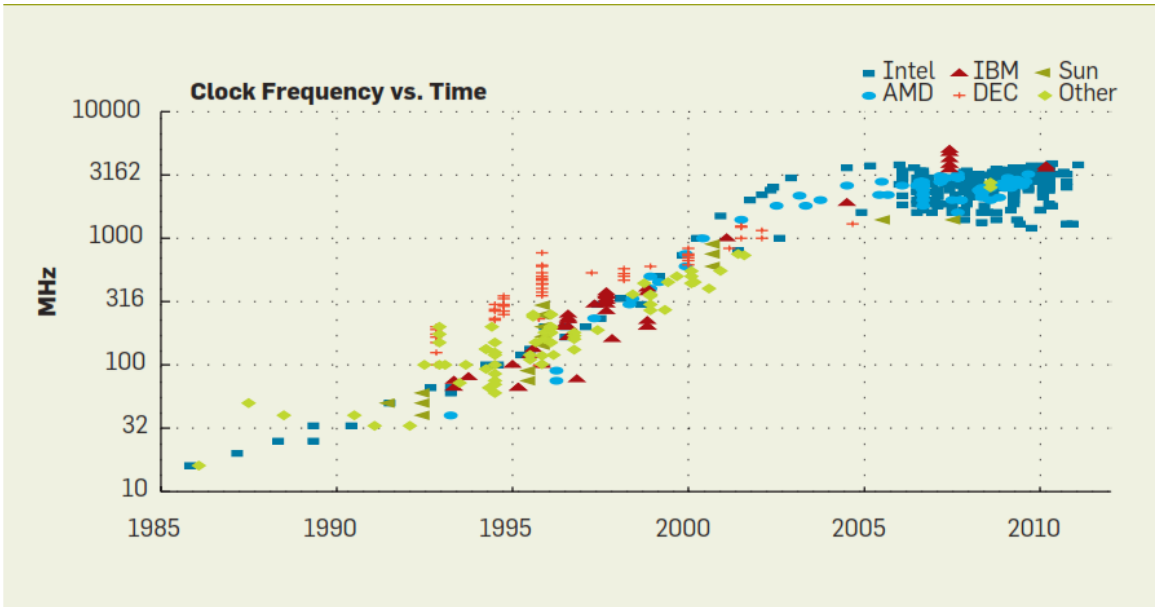


Figure 1.2: Processor frequency over time

Another major challenge is that of power scaling. In early days, power scaling benefited battery life and thereby increased operational time through lower power consumption. While signal power scales down with the supply voltage, noise power remains the same regardless of the power supply voltage. This means that the signal-to-noise ratio (SNR) would decrease with power scaling, degrading both analog and digital circuit performance. Consequently, power scaling may be inhibited unless it is intensely needed by industry. The relationship between the power scaling and the transistor feature size is shown in Figure 1.3 [1].

Even though many analog functional circuit blocks have been replaced by its digital counterparts, switched-capacitor (SC) circuits are still much-used in modern IC industry. They are widely used for discrete-time signal processing applications such as comparators, data converters, amplifiers and filters. Many of their unique characteristics make them suitable for integration into complex, digital-signal-processing blocks with low-cost technology, especially CMOS technology. Advanced CMOS technology increasingly relies on mixed signal processing in which it plays a critical role in establishing connection between analog and digital signal. Because of rapid development in digital signal processing, designers often prefer to process the signal in the digital domain to achieve high efficiency while still relying on analog circuits for receiving and transmitting analog signals. As a result, mixed-signal circuit design is likely to remain an active field in electrical engineering.

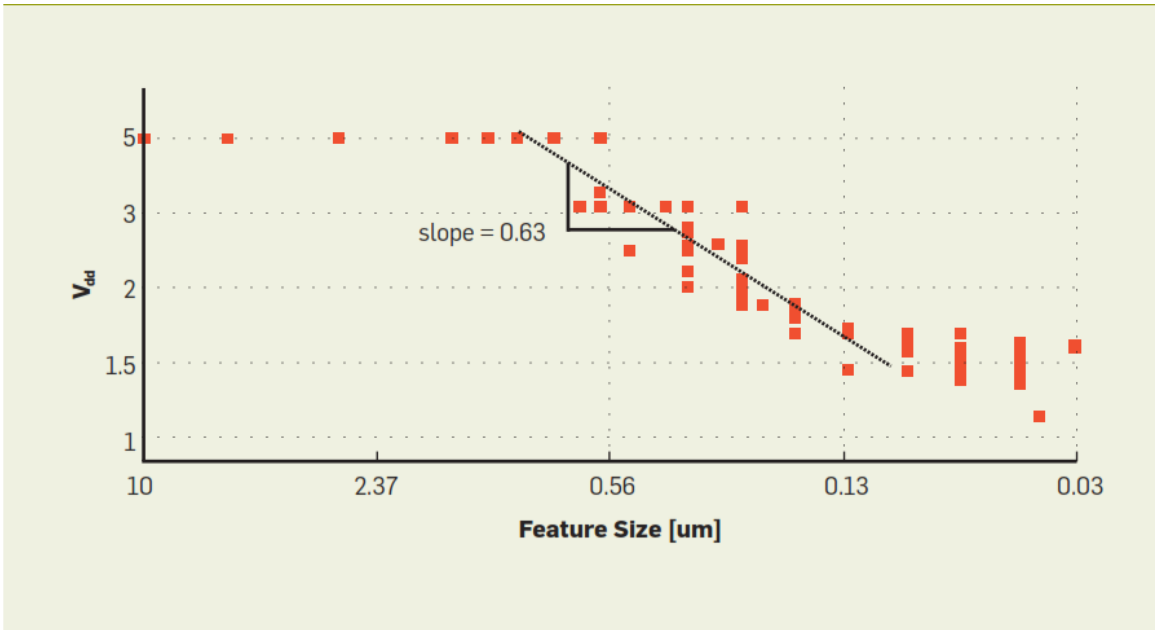


Figure 1.3: Supply voltage vs. feature size

SC circuits use MOS switches, op-amps, and capacitors as their core components. Clock signals are also needed to define each phase. Switched-capacitor approaches have many benefits, including the significant factors of robustness and integration capability. Since highly-integrated systems require smaller feature-size components, often associated with mismatch and

random-variation issues, designers must guarantee accuracy requirements, often by adopting SC circuits. Simulated resistors constructed using switches and capacitors also may produce very large accurate configurable resistance, thereby conserving chip area and guaranteeing the yield.

Since op amps are the only active components in switched-capacitor circuits, op amp performance would most likely largely determine overall switched-capacitor circuit performance. In other words, many challenges in switched-capacitor circuits result from op amp limitations. In op amp design, trade-offs between speed, accuracy, and power dissipation are likely to be major challenges for both contemporary and future designer. For a given structure, circuit speed is proportional to the power consumption. Fast settling performance requires high unity-gain frequency and single-pole op amp transient behavior, while the final settling accuracy is usually determined by the high DC gain. Unfortunately, these two aspects always represent contradictory demands. High DC gain can easily be achieved by cascading transistors or cascading multiple stages, but these strategies suffer from smaller bandwidth and, more importantly, the stability problem. For this reason, frequency compensation is required for two-stage or multistage amplifiers. Many compensation methods based on continuous-time domain [2, 3, 4, 5, 6, 7, 8] have been proposed. Their major target is to extend the gain-bandwidth product as much as possible while still guaranteeing certain stability criteria (usually phase margin). All of these methods were first developed for continuous-time applications and then applied to discrete-time applications (e.g., switched-capacitor circuits). However, there is still a need for a compensation method, especially developed for switched-capacitor use. In addition to the above compensation techniques, slew-rate enhancement (SRE)[9, 10, 11, 12] have also been proposed for improving the large signal op amp performance. When a SC amplifier is operating at large signal levels (e.g., slewing mode), an SRE circuit would automatically turn on and pump current to charge a load capacitance or an internal high capacitive node, resulting in acceleration of the circuit's non-linear large signal response. Another technique, correlated level shifting [20] has been proposed as an accuracy-improvement technique as well as providing the benefit of fast settling performance. However, this technique still has the problem of accuracy/speed trade-off resulting from choosing the size of the correlated level shift capacitor.

In general, the larger the value of the correlated level shift capacitor, the more accurate the output signal level, but at the cost of decreased speed.

This thesis introduces a switched-compensation technique (SCT) that supports both fast settling performance and lower quiescent power consumption. By taking advantage of the initial under-damped ($\xi \ll 1$) rapid estimation phase, the "speed" of switched-capacitor circuits can be enhanced. Detection circuits concurrently begin to detect output signal amplitude and immediately "force" the overall switched-capacitor system back into a critical-damped ($\xi \approx 1$)phase when the output signal amplitude reaches the desired level. By appropriate configuration, the overall system can recover to the desired signal amplitude rapidly with overhead overshoot only and thereby achieve fast settling performance. Because the detection circuits are operating only during the rapid estimation phases, their quiescent power consumption can be conserved. In general, SCT could be applied to any switched-capacitor circuit with piecewise input and output step response. In this thesis, SCT is implemented using a flip-around switched-capacitor amplifier where it performs as a multiplying-digital-to-analog converter (MDAC) like those widely-used in pipeline ADCs. In pipeline ADCs, the first stage MDAC usually determines both the overall data converter's resolution and speed.

1.2 Organization of the thesis

Chapter 2 provides background information for SCT. This chapter first discusses the basics of feedback theory and then provides an overview of general compensation methods such as single Miller compensation and Miller compensation with nulling resistor. Switched-capacitor circuits are also described. As a typical application, the flip-around switched-capacitor amplifier will be discussed along with its implementation as a multiplying-digital-to-analog converter (MDAC). The correlated level shifting (CLS) technique representing material necessary for understanding the proposed switched-compensation technique will also be described.

Chapter 3 provides an SCT overview together with a description of its detailed operation. Several design considerations are discussed, and detection circuitry, including preamplifiers and hysteresis comparators, is explained. Some optimization criteria for preamplifiers are also described.

Chapter 4 describes the SCT detailed overall test bench. Simulation results are presented for the flip-around switched-capacitor amplifier with SCT when compared to a conventional SC amplifier.

Chapter 5 summarizes this thesis and presents its conclusions. Future research idea are also described.

CHAPTER 2. BASIC FEEDBACK THEORY AND REVIEW OF SWITCHED-CAPACITOR CIRCUITS

2.1 Introduction

Feedback is one of the most powerful techniques in the analog circuit design, and the greatest number of interesting phenomena in analog circuit can probably be explained using feedback theory. For example, negative feedback supports high-precision signal processing while positive feedback is responsible for an oscillator's start up condition. Using negative feedback, designers could control circuit input and output impedance and improve the linearity, accuracy performance while also enhancing overall system robustness. However, negative feedback is also a double-edged sword. Among its puzzling drawbacks, stability is the most notorious. Since a loop transfer function is frequency-dependent, "negative" feedback at low frequency might change its polarity at high frequency, resulting in oscillation. An interesting saying related to the perversity of feedback asserts that an op-amp oscillates when we want it to be stable while an oscillator will not start when we want it to oscillate. Up to now, the stability issue still remains one of the most challenging aspects of analog and mixed-signal design.

Since switched-capacitor circuits always incorporate op amps, some sort of feedback configuration network cannot be avoided. Using a capacitor in a feedback network can eliminate op amp loading effects, resulting in large low-frequency loop gain. The feedback ratio sensitivity can also be improved because capacitor-matching can be guaranteed to a much greater accuracy level compared with resistor-matching. As a result, the sample-and-hold application is one of the most attractive uses of switched-capacitor circuits. Through this process, analog input signals can be transferred into the discrete-time domain and subsequently processed by digital circuits.

In this chapter, basic feedback theory will first be reviewed and two classical compensation techniques are re-examined. Classical switched-capacitor amplifier and flip-around switched-capacitor amplifiers are next discussed. Finally, the correlated level shifting (CLS) technique is briefly explained.

2.2 Feedback circuit theory

Figure 2.1 shows a general feedback system [13], in which *H(s)* and *G(s)* are defined as the feed-forward and the feedback networks, respectively. The output signal *H(s)G(s)* of the feedback networks is summed with the input signal, forming *H(s)* input signal. The input signal to *H(s)* is called feedback error and is given by *X(s)* - *H(s)G(s)*. That is,

$$Y(s) = H(s)[X(s) - G(s)Y(s)] \tag{2.1}$$

Thus,

$$\frac{Y(s)}{X(s)} = \frac{H(s)}{1 + G(s)H(s)} \tag{2.2}$$

H(s) is called the open loop transfer function and *G(s)H(s)* is called the loop transfer function.

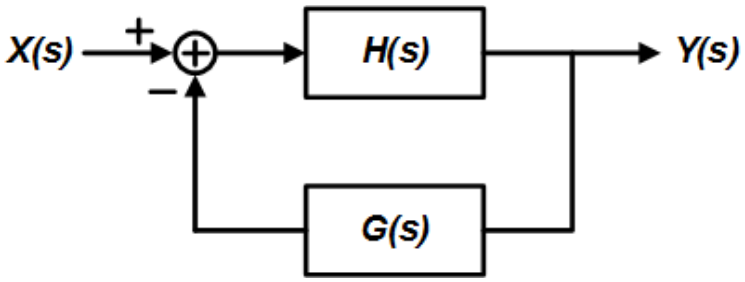


Figure 2.1: Feedback configuration

An intuitive description of the negative feedback configuration is as following. The feedback signal from the *G(s)* output is constantly compared with input signal *X(s)* and produces an error signal unless the feedback signal is identical to the input signal *X(s)*. In other words, the overall system will try to drive the error signal toward zero. In reality, both *G(s)* and *H(s)* are frequency dependent. Usually, the low-frequency characteristic of the feedback configuration

is most sought after. Under that circumstance, *H(s)* and *G(s)* could be denoted as A and β, respectively. A gain "desensitization" effect then takes place. This property can be quantified by 2.3.

$$\frac{Y(s)}{X(s)} \approx \frac{Y}{X} = \frac{A}{1+A\beta} \approx \frac{1}{\beta}(1 - \frac{1}{A\beta}) \tag{2.3}$$

Where we have assumed A$\beta \gg 1$.

We note that the close loop gain is, interestingly, most significantly determined by the feedback factor, β. In other words, even if A deviates by a small fraction, the close loop transfer function could remain almost the same because it dominantly depends on the feedback networks. The important quantity Aβ is called "loop gain". From 2.3, we can see that the higher Aβ, the less vulnerable is the whole close-loop transfer function to variations in A.

Negative feedback also greatly affect the bandwidth of an open-loop system. Here the frequency response of the feed-forward *H(s)* and the feedback *G(s)* networks are taken into account. Assuming that the feed-forward network *H(s)* is a single pole system:

$$H(s) = \frac{A_0}{1 + \frac{s}{\omega_0}} \tag{2.4}$$

Where A_0 denotes the DC gain and ω_0 is the -3dB bandwidth of the open-loop transfer function.

The transfer function of the close loop system is thus,

$$\frac{Y(s)}{X(s)} = \frac{\frac{A_0}{1+\frac{s}{\omega_0}}}{1 + \beta\frac{A_0}{1+\frac{s}{\omega_0}}} = \frac{\frac{A_0}{1+A_0\beta}}{1 + \frac{s}{(1+A_0\beta)\omega_0}} \tag{2.5}$$

The numerator of 2.5 is the same predicted by 2.3. The denominator shows that the -3dB bandwidth has been extended by a factor of $1 + A_0\beta$. Here we should mention that the gain-bandwidth product remains intact. For a first-order system, the speed (transient response) is determined by the gain bandwidth product. For example, if the input signal is a step function, the output transient response will be approximately:

$$Y(t) = 1 - e^{A_0\beta}t \tag{2.6}$$

In real word, feedback analysis for circuit design can be very complicated. For example, if feedback networks *G(s)* in Figure 2.1 are bi-directional networks, the close loop transfer

function will become more complex, making intuitive analysis impossible. Feedback circuit analysis and design may therefore become extremely tedious if transistor's parasitic effects are taken into account.

Negative feedback has been applied into virtually every analog circuit design, because its prosperities of suppressing non-ideality and variation have won favor from designers. However, feedback systems also suffer from a potential critical problem, i.e., instability.

Generally, the feedback network is designed to be frequency-independent so that the above mentioned merits of negative feedback can be achieved. A feedback networks $G(s)$ can be represented by β as shown in figure 2.2. The transfer function can be expressed as:

$$\frac{Y(s)}{X(s)} = \frac{H(s)}{1 + H(s)\beta} \tag{2.7}$$

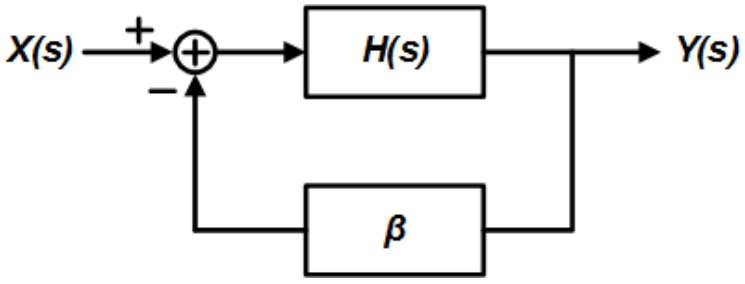


Figure 2.2: Negative feedback system

If $H(j\omega_o)\beta = -1$, the denominator from 2.7 goes to zero and thus the overall transfer function becomes infinite. This result reveals the probability of system oscillation. The condition for oscillation can be expressed as

$$|H(j\omega_o)\beta| = 1 \tag{2.8}$$

$$\angle H(j\omega_o)\beta = 180^\circ \tag{2.9}$$

Equations 2.8 and 2.9 are well-known as "Barkhausen's Criteria". It is clear that at ω_o the total phase shift of the loop is 360° because the negative feedback itself has already introduced a 180° phase shift, so if the system satisfies Barkhausen's Criteria, any small excitation (e.g., noise or power supply variation) within the circuit will result in oscillation. As mentioned earlier, $H(s)\beta$ represents the loop gain, so system stability can be determined by the loop's

frequency response. This leads to the concept of phase margin. If the system is a minimum-phase system and $|H(j\omega_o)| \gg 1$, then the system is unstable.

The above analysis is based on a first order (single-pole) system. However, in the real world, circuits are generally higher order (usually more than two poles) systems. For high order system, it is difficult to use intuitive method to analyze transient behavior. A general method is to simplify high order systems into second-order systems because such systems have been comprehensively and easily understood [29] and can often serve as good approximations of higher-order systems.

2.3 Frequency compensation techniques

Since the op amps are usually developed as multiple stage circuits and thus they can be regarded as high order systems. There is no doubt that multiple stage op amp will often suffer from stability problem because of their negative feedback configuration. A worst case occurs when the feedback factor $\beta = 1$ (assuming no frequency dependency). Even though the feedback factor is usually smaller than one in a switched-capacitor application, a stable unity-gain buffer connection is still required. A high order system corresponds to existence of multiple poles. Typically, if no corrective action is taken for a multi-stage amplifier, these poles might be very close to one another and thus threaten system stability. The amplifier thus must be "compensated", meaning that we should separate the non-dominate poles to frequency as high as possible. Traditional design experience suggests that the second dominate pole should be placed away from the unity gain frequency by a factor of two. Moreover, the higher-order poles and zeros should also be avoided to guarantee a good phase margin. Several compensation methods have been proposed over the past several decades [2, 3, 4, 5, 6, 7, 8]. Among them, Miller compensation is the most widely-used method in analog circuit design. In this section, single Miller compensation (SMC) and Miller compensation using a nulling resistor will be discussed.

2.3.1 Single Miller compensation

Single Miller compensation is the simplest compensation method, accomplished by introducing a capacitor. Its behavior diagram is shown in Figure 2.3 where A_1 and A_2 represent first and second stage gains and C_c represents the compensation capacitor. While the structure shown on the plot is a single-ended version, this concept can also be applied to fully-differential structure.

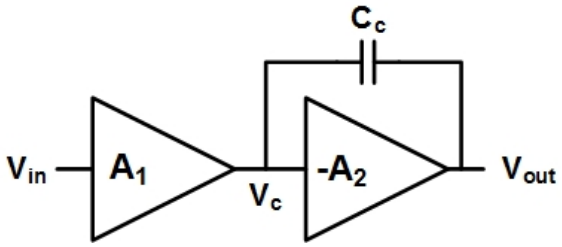


Figure 2.3: Single Miller compensation

Without Miller capacitor, the first and second dominate poles are give as $p_i = \frac{1}{R_i C_i}$, where R_i and C_i represent the each stage's output node capacitance and resistance. Usually, these two poles are very close to each other. This results in stability issue because of a -180° phase lag before the unity gain frequency. In order to achieve pole splitting effect, a Miller compensation capacitor is added across a negative gain stage. By taking advantage of the Miller effect, the capacitance seen at the internal node is amplified by a factor of $(1+A_2)$. Thus, the effective capacitance at the node V_c is $(1+A_2)C_c$. This reveals that the location of the first pole is pushed to a much lower frequency if negative gain is high. Further more, the non-dominate pole at the output node is also pushed to higher frequency. But the phenomenon of the second pole splitting effect will saturated when C_c increases. Thus, further increasing the compensation capacitor only push the dominate pole to lower frequency.

The Miller capacitor, however, also introduces a right half plane (RHP) zero. Because the compensation capacitor will provide a capacitive signal path, i.e., will be "shorted" at high frequencies, two feed-forward signal paths in opposite direction will create an RHP zero that further deteriorates the phase margin.

The small-signal model for the two-stage op amp is shown in Figure 2.4. The small-signal

transfer function for two-stage amplifier with Miller compensation is given by

$$\frac{V_{out}}{V_{in}}(s) = \frac{g_{m1}R_1 g_{m2}R_2(1-\frac{s}{z_1})}{(1-\frac{s}{p_1})(1-\frac{s}{p_2})} \tag{2.10}$$

Where p_1, p_2 and z_1 are located at

$$p_1 = -\frac{1}{R_1 g_{m2} R_2 C_c} \tag{2.11}$$

$$p_2 = -\frac{g_{m2}C_c}{C_c C_1 + C_c C_2 + C_2 C_1} \approx -\frac{g_{m2}}{C_2 + C_1} \tag{2.12}$$

$$z_1 = \frac{g_{m2}}{C_c} \tag{2.13}$$

The open-loop gain for this amplifier is $A_0 = g_{m1}g_{m2}R_1R_2$ and the gain-bandwidth product is given as GBW $= \frac{g_{m1}}{C_c}$. Because of the characteristic of the RHP zero, the phase margin of the loop might fall below zero and result in a stability problem. Since this RHP zero is dependent on the compensation capacitor, further pushing the dominant pole toward origin by increasing C_c provides little help with respect to stability. Many other techniques [2, 3, 8] have been proposed to eliminate this RHP zero, e.g., blocking this feed-forward current, providing another opposite-polarity feed-forward current path, or feeding back compensation current from a low impedance node.

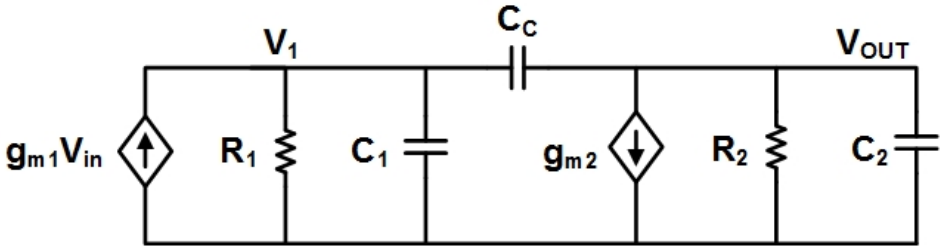


Figure 2.4: Small signal model for Miller compensation

2.3.2 Miller compensation with nulling resistor

Since single Miller compensation suffers from the problem of RHP zero, adding a resistor in serial with the compensation capacitor helps to block the feed-forward signal path at high frequency, so the zero would move. The block diagram and small-signal model for Miller

compensation with a nulling resistor is shown in Figure 2.5.

With the additional nulling resistor, the location of the zero is given by:

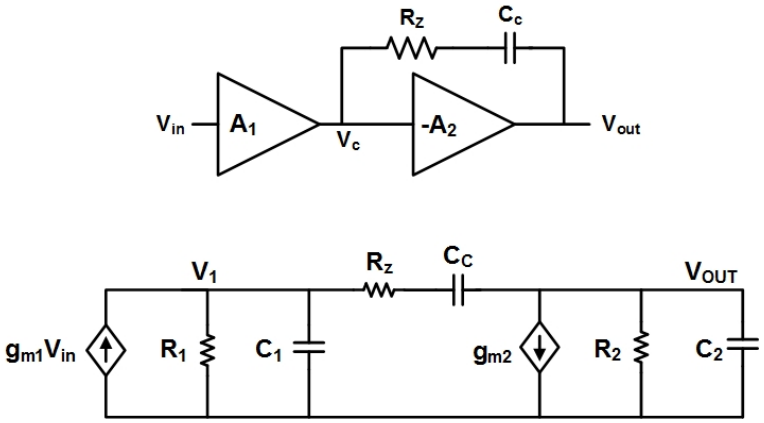


Figure 2.5: Miller compensation with nulling resistor

$$z_1 = \frac{1}{(\frac{1}{g_{m2}} - R_z)C_c} \tag{2.14}$$

From 2.14, we can observe that the location of the zero can be controlled by a nulling resistor R_z. If the value of the nulling resistor is set to be $R_z = \frac{1}{g_{m2}}$, this zero will move to infinity. In addition, by further increasing this R_z, the previous RHP zero can be transferred into the left half plan (LHP) zero and improve the phase margin. However, this nulling resistor also introduces another pole located at $p_4 = \frac{1}{R_z C_1}$. Typically, the value of R_z cannot be too large to prevent this pole from moving to a lower frequency.

2.4 Switched-capacitor circuits

The switched-capacitor (SC) circuits were first conceived in Maxwells treatise in 1873. He first described about galvanometer swinging back and forth and transferring condensers and current; this is the same basic method of operation used in switched-capacitor circuits. In modern times, three University of California at Berkeley researchers, Paul Grey, David Hodges and Robert Brodersen, introduced switched-capacitor circuits into the academic and industrial fields. First generation switched-capacitor circuits, including A/D converter, op amps and filters were first implemented into telephone system .

The first application of a switched-capacitor circuit was a filter. High-performance analog filters can be realized using passive RLC circuits. In the early 1960s, designers began to use active RC filters to eliminate the large area occupied by the inductor [21]. Active RC filters were first constructed using op-amps, chip capacitors and resistors. During that time, the value of MOS capacitors were typically less than 100 pF, so the resistors used in the filter had to be very large to achieve low cut-off frequencies. The absolute achieved accuracy value for each capacitor and resistor was only 5-10 percent, resulting in a poor-controlled overall RC constant value(up to 20 percent deviation) after fabrication [24]. This error was further deteriorated by temperature and signal level variation. To overcome these difficulties, simulated resistor constructed with capacitors and switches replaced the traditional resistor [22, 28, 30]. Since the simulated resistor value is determined by the capacitor value and the clock frequency, the time constant of the filter is therefore determined by the capacitor ratio and the clock frequency. The clock can be very precisely generated by a crystal while the capacitor ratio can be accurately controlled by proper matching at a 0.1-0.5 percent level. This characteristic is actually more critical when building a high-order band-pass filter requiring a high quality factor at its center frequency [25]. This property also is beneficial to robustness with respect to temperature and aging. For these reasons, the sampled-data technique realized using switched-capacitor filters can be used to economically and accurately model their active RC counterparts in the analog domain. The advantage of switched-capacitor approach is that a previously-developed active RC biquad filter can be implemented on a chip. These merits enable a new generation of switched-capacitor filters to replace all but the most esoteric of active RC filter designs [23].

The potential for low cost [27] has encouraged engineers to develop design technique for realization of precision high-linearity switched capacitor (SC) stages constructed entirely from MOS transistors. Using MOSFET as capacitor is appealing because the chip area associated with traditional capacitors can be reduced. The advantages are: the thin oxide itself already provides larger capacitance per unit area than that of a poly-poly or a metal-metal capacitor. The latest technology processes also minimize random capacitance variation. Finally, the ratio between parasitic capacitance and the main capacitance realized by a MOS capacitor is usually smaller than that in a conventional approach [26].

Data converters have become increasingly popular in many applications where higher bandwidth and sampling speeds are required, such as in software-defined radios [31]. For applications in well-behaved environments, such as wire-line applications, more and more front-end tuners have been replaced by a data-converter and a very simple front-end consisting of little more than a low-noise (sometimes programmable) amplifier and possibly some simple low-pass filters. Almost all contemporary data converters use switched-capacitor circuits for high resolution. This demand has stimulated designers to focus on designing high-performance switched-capacitor circuits, especially SC amplifiers. In this section, a unity-gain sampler, a non-inverting switched-capacitor amplifier and a flip-around switched-capacitor amplifier will be discussed along with the correlated level-shifting technique.

2.4.1 Unity gain sampler

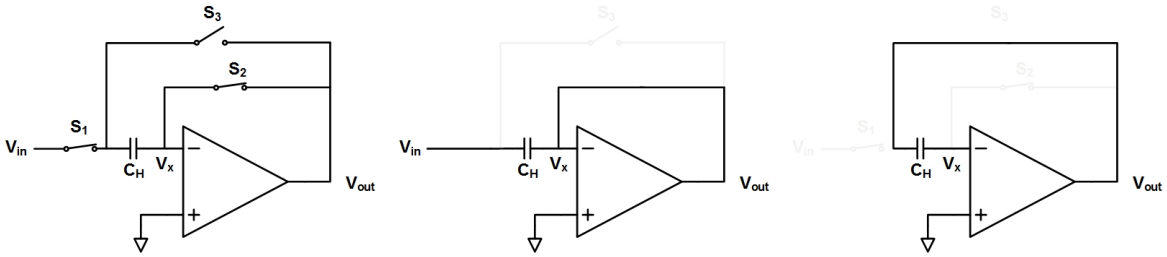


Figure 2.6: (a)Unity-gain sampler,(b)sampling mode,(c)amplification mode

Because of the characteristics of a switched-capacitor when used a resistor, a unity-gain amplifier can be built using switched-capacitor components. Figure 2.6(a) depicts the topology for a unity-gain sampler using switched capacitors. Three switches control the operation of sampling and amplification. In the sampling mode, S_1 and S_2 are on and S_3 is off. The sampling schematic is shown in Figure 2.6(b). In amplification mode, S_1 and S_2 are off and S_3 is on, placing the capacitor C_H across the op amp's inverting input node and output node, as shown in Figure 2.6(c). Since an ideal op amp should "force" V_x to virtual ground and charges on the C_H should remain the same, the output of op amp should "track" the input signal until the unity-gain sampler samples once again.

Several design considerations are related to the importance of timing control. S_2 should turn off slightly before S_1 does. When S_2 turns off, there is no signal path at the inverting input of the op amp, keeping the charges on the capacitor plate constant. In other words, even though there exists a charge redistribution (due to S_1 turn-off) on the other capacitor plate, these charges will not be sampled on the C_H. So S_2 plays the most critical role with respect to charge injection issue. In addition, the charge injected by the S_2 will only affect the DC offset of the final value. This charge-injected value can be approximately calculated by $\Delta q_2 = WLC_{ox}(V_{DD} - V_{TH} - V_X)$. Since V_X is about at virtual ground for large loop gain, this charge injection is virtually constant.

2.4.2 Non-inverting switched-capacitor amplifier

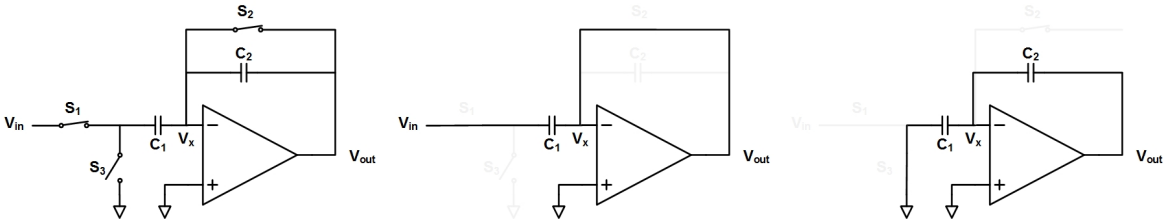


Figure 2.7: (a)Non-inverting amplifier,(b)sampling mode,(c)amplification mode

The non-inverting switched-capacitor amplifier provides a configurable feedback networks. Thus, the gain of the switched-capacitor amplifier can be set by its feedback capacitor C_1 and C_2. Figure 2.7 shows the schematic of the non-inverting structure. In the sampling mode, S_1 and S_2 are turned on and S_3 is turned off. The amplifier is connected as a unity-gain buffer and thus its inverting input node is at virtual ground. The input signal would be sampled on C_1. When the sampling mode is completed, S_2 turns off first followed by S_1 turning off and S_3 turning on. The output signal amplitude would changes from zero to approximately $\frac{C_1}{C_2}V_{in}$. So the non-inverting switched-capacitor amplifier has a gain of $\frac{C_1}{C_2}$. The sequential time arrangement for the amplification phase mentioned above is considered for minimizing the charge- injection issue. By blocking the signal path from the inverting input node, charge-injection issue can be suppressed.

2.4.3 Flip-around switched-capacitor amplifier

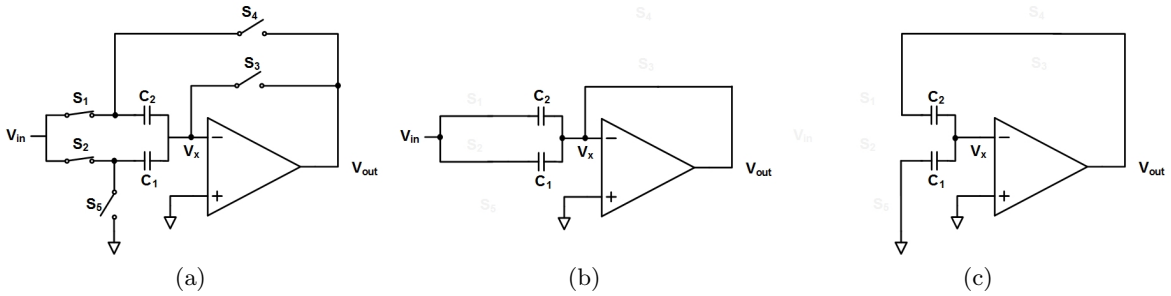


Figure 2.8: (a)Flip-around switched-capacitor amplifier,(b)sampling mode,(c)amplification mode

The flip-around switched-capacitor amplifier is also known as "multiply-by-two" amplifier. This topology achieves benefits of higher speed and low gain error. The schematic is shown in Figure 2.8. The amplifier usually incorporates two equal capacitors $C_1 = C_2 = C$ to realize a gain of two. In sampling mode, the circuit is configured as in Figure 2.8(b) by causing the inverting input of the op amp V_x to be virtual grounded. During this time, these two capacitors track the input signal. When the amplification phase begins, the op-amps will try to "force" the non-inverting input node to virtual ground. In other words, the op amp transfers all the charges from C_1 to C_2 and at the same time charges or discharges the load capacitor according to the input signal. Since both C_1 and C_2 have the same values, the gain of this flip-around switched-capacitor amplifier is two. The timing control illustrated for this topology is similar to the previous two topologies. In the transition from sampling mode to amplification mode, S_3 turns off first. The charge injected by S_1 and S_2 and absorbed by S_4 and S_5 is not critical. S_3 will introduces an error but it can be regarded as a constant offset and this offset can be suppressed by differential operation.

If the finite loop gain is taken into consideration, the actual gain of the flip-around switched-capacitor amplifier is given by 2.15 where T is the loop gain during the amplification phase.

$$V_{out} = V_{in}(1 + \frac{C_1}{C_2})(\frac{1}{1 + \frac{1}{T}}) \tag{2.15}$$

From 2.15, we know that the accuracy of the final settled value can be improved with higher op amp loop gain. However, higher loop gain would represent a stability issue as mentioned

earlier. Compensation is also a critical factor for high loop gain to guarantee stability. Also, when the output signal amplitude reaches the rail, the op amp loop gain will suffer degradation and reduce the accuracy of the switched-capacitor amplifier.

2.5 Correlated level shifting technique

Correlated level-shifting (CLS) has been introduced as an accuracy improvement technique [20]. It reduces op amp errors due to the finite gain, especially at rail to rail output when the overall loop gain is the lowest. CLS requires an extra clock and a level-shift phase in addition to the conventional two-clock operation.

As mentioned earlier, the op amp loop gain would drop when the output signal amplitude reaches the rail. In other words, the inverting input of the op amp is not virtually grounded but is given by 2.16.

$$V_x = V_{out}\frac{1}{A} \tag{2.16}$$

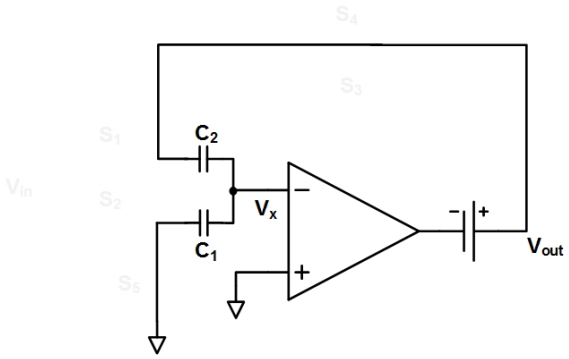


Figure 2.9: Switched-capacitor amplifier with level shifting battery

One possible solution to this problem would be to insert a battery (usually implemented using a charged capacitor) between the output of the op amp and the overall output at the amplification phase so that the output of the op amp is set as close as possible to its quiescent DC value while still maintaining the output signal 2.9. Consequently, the inverting input of the op amp behaves more like virtual ground and the loop gain requirement can thus be relaxed.

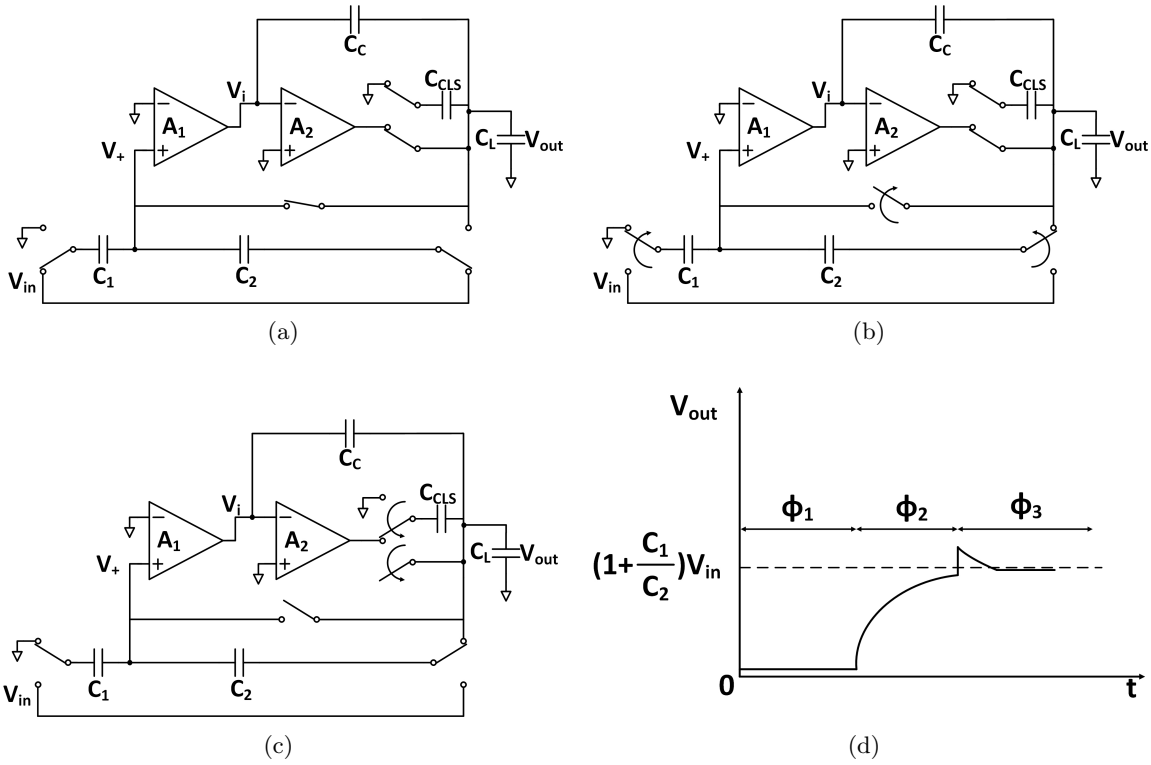


Figure 2.10: Switched-capacitor amplifier with CLS, (a)Sampling mode, (b)Estimation mode, (c)Level shifting mode, (d)Waveform at the load

The above solution can be realized using correlated-level shifting capacitor. The overview of the CLS operation is shown in figure 2.10 where the core amplifier incorporates a two stage amplifier with Miller compensation. The three phases are sampling, estimation and level shifting. The first two phases are the same as for the conventional switched-capacitor amplifier described in the previous chapter. During these two phases, an additional capacitor C_{CLS} is connected in parallel with the load capacitor. At the beginning of the level shift phase, C_{CLS} is connected between the output of the op amp and the overall output. If the parasitic capacitance of the second stage is negligible, this level shift capacitor would force the second stage of the op amp to ground (or middle of the rail) while the overall output remain the same. In reality, because of the parasitic capacitance of the second stage op amp, the second stage of the op amp cannot be set to ground and thus overall output will suffer from a voltage jump as shown in 2.10(d).

The connection of the compensation capacitor is also critical. For conventional flip-around switched-capacitor amplifiers, the compensation capacitor is always connected between the second negative gain stage if single Miller compensation is used. However, for the correlated level-shifting case, the loop gain of the flip-around switched-capacitor amplifier would change after the level shift phase. The loop gain comparison between the estimation phase and the level-shift phase is given by 2.17.

$$T_{EST} = T_{CLS}(\frac{C_{CLS}}{C_L + C_{CLS} + C_{fb}}) \tag{2.17}$$

Where T_{EST} and T_{CLS} represent the op amp loop gain during estimation phase and level-shift phase, respectively. C_{CLS} is the correlated level-shift capacitor and C_L is the load capacitor. C_{fb} denotes the equivalent feedback capacitor as seen from the overall output node.

Since we want the phase margin both before and after the level-shift phase to be the same, the Miller effect should, together with their loop gain counterpart, suffer from the decreased factor given by 2.17. As a result, the compensation capacitor is connected between the second stage input and overall output after the level-shift phase to achieve the same settling performance.

CHAPTER 3. SWITCHED-COMPENSATION TECHNIQUE

3.1 Introduction

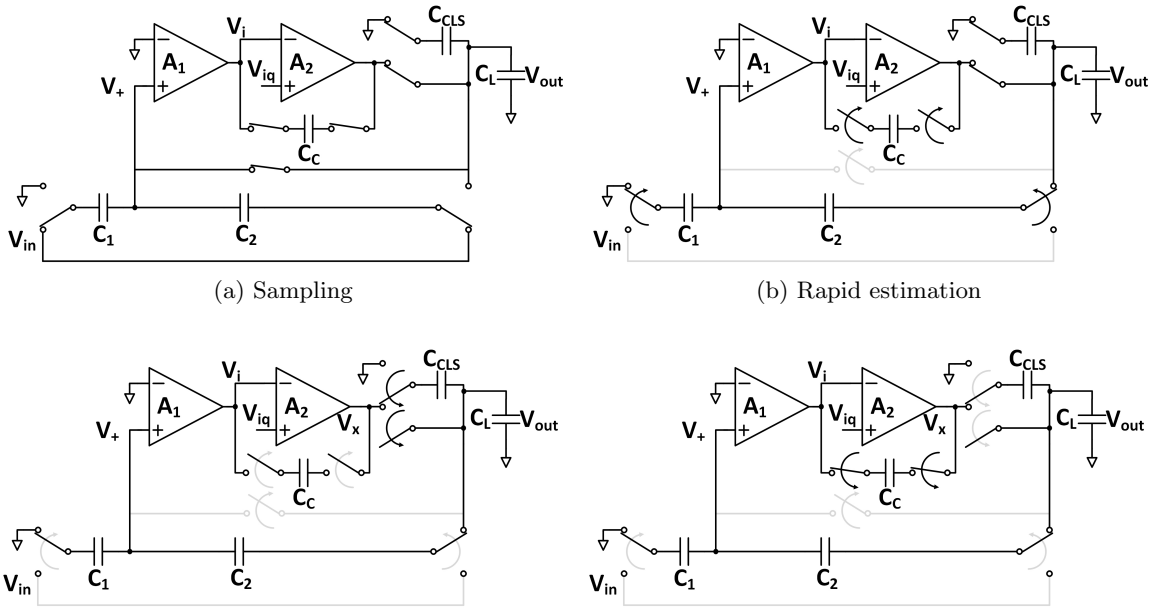
This chapter will introduces switched-compensation technique (SCT). As mentioned earlier, the speed of the switched-capacitor amplifier depends mainly on the performance of the op amp itself. Many methods [15, 16, 17] have been proposed to achieve shorter settling time for the switched-capacitor circuit application by optimizing the settling behavior of the op amp. The conventional approach has been to design an operational amplifier to first meet the DC gain requirement, then try to increase the bandwidth as much as possible while still guaranteeing appropriate phase margin. While adaptive biasing or slew-rate enhancement [9, 18, 19] has been used to improve the transient response of the amplifier, this works only in slewing or large-signal situations. In general, these methods spared no effort to build a good op amp so that settling time could be minimized. Correlated level-shifting [20] is a technique to improve settling time by revising the switched-capacitor architecture and still preserve an equivalent high DC gain, but there still is a speed/accuracy trade-off in choosing the size of CLS capacitor.

The switched-compensation technique (SCT) allows faster settling performance and lower quiescent power consumption. A design example describing a flip-around switched-capacitor amplifier will be given here. By taking advantage of the initial under-damped ($\xi \ll 1$) rapid estimation phase, the "speed" of the switched-capacitor amplifier can be enhanced. At the same time, the detection circuits begin detecting the output signal level and immediately "force" the overall switched-capacitor system back to a critically-damped state ($\xi \approx 1$) when the desired output signal level is reached. By appropriate configuration, the overall system can rapidly recover to the right signal level with tolerable overshoot and thereby achieve faster settling performance.

3.2 SCT applications

SCT is a technique that enhances the settling process and reduces the quiescent power consumption. In general, SCT could be applied to any switched-capacitor circuit with piecewise input and output step response. In this paper, SCT is implemented as a first-stage multiplying-digital-to-analog converter (MDAC) of a pipeline ADC in which the first stage MDAC limits both the accuracy and maximum operating speed of the entire ADC.

3.3 SCT operation



(a) Sampling

(b) Rapid estimation

(c) Level-shifting

(d) Critically-damped

Figure 3.1: Four phases of the switched-compensation technique (SCT)

Since SCT could resolve the dilemmas related to speed and accuracy, it would be much more preferable to implement it as a multi-stage amplifier where high DC gain and large gain-bandwidth product could be easily achieved (ignoring stability concerns that can be addressed by SCT). One design example of a two-stage operational amplifier with SCT is shown in Figure 3.1. There are four phases: 1) sample the input signal with C_1 and C_2, 2) rapidly approach the desired signal level by disconnecting the compensation capacitor C_c from the op amp, 3)

use a level-shifting capacitor C_{CLS} to prepare for the critically-damped phase, 4) switch to a critically-damped configuration by connecting the compensation capacitor back into the op amp. Note that this operation is similar to the three-phases CLS technique [20] used in the MDAC except the operation of the compensation capacitor.

Figure 3.2 shows the anticipated waveform at the output with and without SCT. Assume that the system exhibits a second-order system response with the same nature frequency ω_n but a different damping ratio ξ. With the SCT, the rapid estimation phase would behave like an under-damped response. Then, after the level-shifting and critically-damped phase, the output signal waveform would quickly settle to the desired value. In reality, a poorly-compensated op amp usually has a higher ω_n than a well-compensated op amp exhibiting the same power consumption. The rapid estimation phase will have faster response than shown on the plot and thus a much shorter settling time is thus expected.

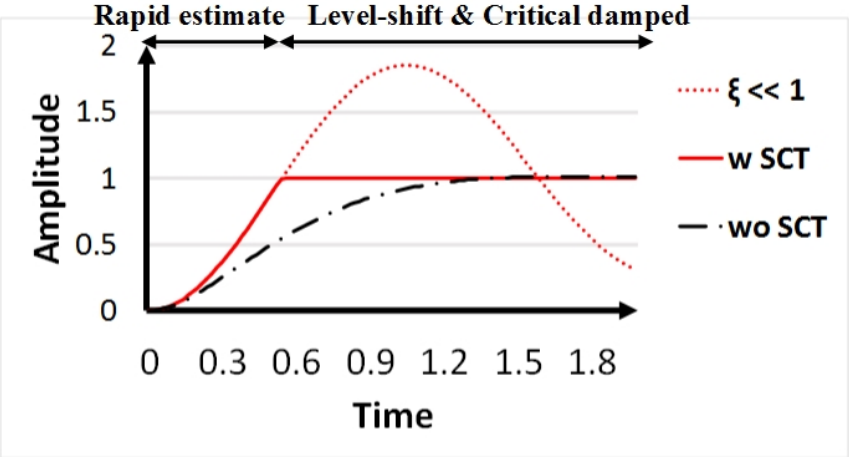


Figure 3.2: Anticipated transient response of SCT

3.4 SCT design consideration

There might be several questions regarding the SCT: 1) why is a level-shifting phase needed before the critically-damped phase? 2) how is timing control for each phase? 3) what are the appropriate sizes for the level-shifting capacitor and the compensation capacitor?

Before answering these questions, a clear understanding of how an under-damped SC circuit behaves is required. Since we want to "force" a second-order system to transition from an under-damped situation to a critically-damped situation, every high impedance node in the system should be immediately set to each settled final signal level as accurately as possible. Otherwise, a long recovery time would make the initial fast-approaching response useless. At the beginning of the rapid estimation phase, the compensation capacitor is disconnected from the SC amplifier while the other parts still conform to a conventional flip-around connection. Following this phase, the DC quiescent voltage difference between the second stage input and output is sampled by the compensation capacitor. During the rapid-estimation phase, charges on the two feedback capacitors C_1 and C_2 transfer from one to the other following the law of charge conservation. If we neglect non-ideal effects (including charge loss, amplifier offset and finite amplifier gain), the output node of the op amp can be expressed by:

$$V_{out}(t) = [1 + \frac{C_1}{C_2}]V_{in}(t) + [1 + \frac{C_1}{C_2}]V_+(t) \tag{3.1}$$

Where C_1 and C_2 are feedback capacitors. V_+ is the non-inverting input of the first-stage op amp and V_{out} is the SC amplifier output.

Ideally, if the system settles down, V_+ should be virtually-grounded and V_{out} would reach the desired value. Even if the whole system hasn't settled down (e.g., due to ringing), V_+ should be zero when V_{out} reaches its desired amplitude value as a consequence of the charge conservation law. Consequently, the zero-crossing of the V_+ is a good indicator for determination as to whether or not the output has reached the desired value. Ideally, we want to "stop" the overall system at the point where the output reaches its desired value. In addition, at that instant, the voltage of internal high impedance nodes (V_i in the example above) differ if the system is under-damped. If this internal node voltage can be set to the final settled voltage value and the overall system's damping factor modified to the appropriate value (e.g., ξ=1) instantaneously, we would expect that SC circuit would settle immediately and a shorter settling time achieved.

Therefore, SCT is designed for setting the internal nodes voltage to the final settled value as accurately as possible while keeping other node voltages intact. This is realized by first using correlated level shifting. A schematic diagram and variables are shown in Figure 3.3 where

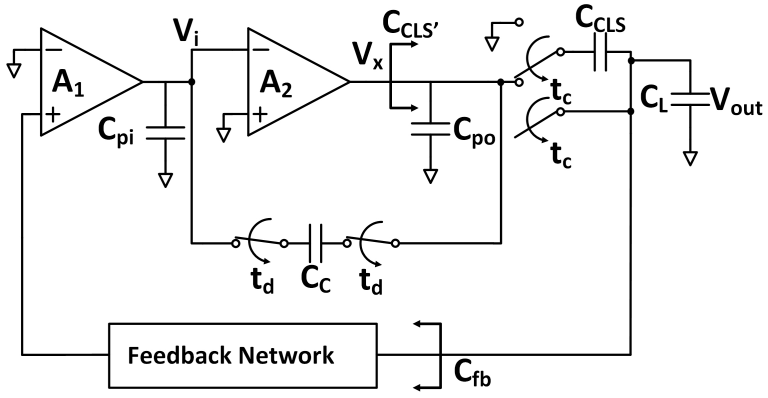


Figure 3.3: Level-shifting and critically-damped phase

the parasitic capacitance of the internal node and the output node of the op amp are labelled as C_{pi} and C_{po}, respectively. t_c and t_d represent the times of the level-shifting phase and the critically-damped phase. The op amp's output node voltage V_x and overall output node voltage V_{out} before and after the level-shifting phase can be calculated by:

$$C_L(V_{out}|_{tc^-} - V_{out}|_{tc^+}) + C_{CLS}[V_{out}|_{tc^-} - (V_{out}|_{tc^+} - V_x|_{tc^+})] + (C_{fb})(V_{out}|_{tc^-} - V_{out}|_{tc^+}) = 0 \quad (3.2)$$

$$C_{po}(V_{out}|_{tc^-} - V_{out}|_{tc^+}) + C_{CLS}[-V_{out}|_{tc^-} - (V_x|_{tc^+} - V_{out}|_{tc^+})] = 0 \quad (3.3)$$

From 3.3, expression can be simplified into

$$(C_{po} + C_{CLS})V_x|_{tc^+} = (C_{po} - C_{CLS})V_{out}|_{tc^-} + C_{CLS}V_{out}|_{tc^+} \quad (3.4)$$

$$V_x|_{tc^+} = \frac{C_{po} - C_{CLS}}{C_{po} + C_{CLS}}V_{out}|_{tc^-} + \frac{C_{CLS}}{C_{po} + C_{CLS}}V_{out}|_{tc^+} \quad (3.5)$$

Plug 3.5 into 3.2

$$V_{out}|_{tc^+} = \frac{C_L + C_{CLS} + C_{fb} + \frac{C_{CLS}(C_{po}+C_{CLS})}{C_{po}+C_{CLS}}C_{CLS}}{C_L + C_{CLS} + C_{fb} - \frac{{C_{CLS}}^2}{C_{po}+C_{CLS}}C_{CLS}}V_{out}|_{tc^-} \quad (3.6)$$

Rearranging 3.6 will give

$$V_{out}|_{t_c{}^+} = (1 + \frac{1}{\lambda})V_{out}|_{t_c{}^-} \quad (3.7)$$

$$V_x|_{t_c{}^+} = (\frac{C_{po} + \frac{C_{CLS}}{\lambda}}{C_{po} + C_{CLS}})V_{out}|_{t_c{}^-} \quad (3.8)$$

$$\lambda = \frac{C_L}{C_{CLS}} + \frac{C_L}{C_{po}} + \frac{C_{fb}}{C_{po}//C_{CLS}} + 1 \quad (3.9)$$

Where C_{CLS} is the correlated level-shift capacitor and C_{fb} is the feedback capacitance looking into the feedback network.

If we make $\lambda \gg 1$ by minimizing the parasitic capacitance on both internal and output nodes, 3.7 and 3.8 could be further simplified into:

$$V_{out}|_{t_c{}^+} \approx V_{out}|_{t_c{}^-} \tag{3.10}$$

$$V_x|_{t_c{}^+} \approx 0 \tag{3.11}$$

From 3.10 and 3.11, we know that the output node still holds that desired value at that instant and the op amp output V_x after the level-shifting phase would be set immediately to ground or the middle of the rail. Phase four (critically-damped phase) takes place immediately after the level- shifting phase by connecting the compensation capacitor back into the op amp. The internal node voltage V_i and op amp's output node voltage V_x before and after the critical-damped phase could be calculated from:

$$C_{pi}(V_i|_{t_d^-} - V_i|_{t_d^+}) + C_c[V_c - (V_i|_{t_d^+} - V_x|_{t_d^+})] = 0 \tag{3.12}$$

$$(C_{po} + C_{CLS'})(V_x|_{td^-} - V_x|_{td^+}) + C_c[-V_c - (V_x|_{td^+} - V_i|_{td^+})] = 0 \tag{3.13}$$

Where V_c is the voltage difference sampled on the compensation capacitor after the sampling phase and $C_{CLS'}$ is the capacitance looking into the CLS capacitor. If we assume that there is no charge loss from the compensation capacitor, then the voltage difference is just the quiescent voltage difference between the second stage input and output node. Thus, $V_c = V_{iq} - V_{oq} = V_{iq}$. Thus, 3.12 can be expressed as

$$V_x|_{td^+} = \frac{C_{pi}}{C_c} V_i|_{td^-} - (1 + \frac{C_{pi}}{C_c}) V_i|_{td^+} + V_{iq} \tag{3.14}$$

Combining 3.13 and 3.14, we obtain

$$V_i|_{t_d{}^+} = (\frac{\frac{C_{pi}}{C_c}}{1 + \frac{C_{po}+C_{pi}+C_c}{C_{CLS'}+C_c}}) V_i|_{t_d{}^-} + (\frac{1}{1 + \frac{C_{po}+C_{pi}+C_c}{C_{CLS'}+2C_c}}) V_{iBias} - (\frac{1}{1 + \frac{C_{po}+C_{pi}+2C_c}{C_{CLS'}}}) V_x|_{t_d{}^-} \tag{3.15}$$

Where V_{iBias} is the quiescent voltage of the internal node.

If we continue to assume that the parasitic capacitance on both internal and output nodes are negligible, 3.15 could be further simplified into:

$$V_i|_{t_d{}^+} \approx V_{iBias} \tag{3.16}$$

The internal node V_i would be pulled back to its quiescent value that is very close to its final desired settled value (after the level-shifting phase, V_x could ideally be set to zero and thus the second stage input voltage would equal its quiescent voltage level). Meanwhile, the output node of the op amp V_x remains unchanged. With the compensation capacitor, the overall system's damping factor could be instantaneously set to the appropriate value. In reality, even though tiny deviation may still exists right after phase four, the overall system would still settle much faster than in the conventional case.

Clock phases one and two are determined by the external clock frequency. Clock phase four follows immediately after phase three by adding a small delay. The trigger for clock phase three could be determined from the zero-crossing of the op amp feedback input because that is the time when both input and output reach their desired signal levels. The detection circuit could be built by a high speed comparator only operating during the rapid estimation phase. For this reason, the detection circuit consumes only dynamic power.

After the level-shifting phase, the loop gain of the SC circuit can be approximated by

$$T_{phase3} = \frac{C_{CLS}}{C_{CLS} + C_L + C_{fb}} T_{phase2} \tag{3.17}$$

Where T_{phase2} and T_{phase3} represent the loop gains during the rapid estimation phase and the level-shifting phase.

Since the CLS capacitor is determined by the accuracy requirement for the MDAC [20], 3.17 anticipates that the compensation capacitor could be reduced by at least the factor reduced by the loop gain. As a result, the compensation capacitor used in SCT is different from a traditional SC amplifier with CLS.

3.5 Detection circuits

The detection circuits can be built using a high speed comparator. There have two requirements. The first is that they should react to the zero-crossing input signal as quickly as possible. In other words, the delay time should be minimized. The general method for minimizing the delay time is to use a chain of preamplifiers. Another one is from robustness consideration. The detection circuits are also vulnerable to noise problem, resulting in error in

triggering the level-shifting and critically-damped phase. Consequently, it is necessary to add a hysteresis comparator after a chain of preamplifiers. The hysteresis comparator's upper and lower threshold region is determined by the robustness requirement. The schematic diagram of detection circuit is given in Figure 3.4. Since this chain of preamplifiers should be configured for minimizing delay time while still guaranteeing robustness of the zero-crossing detection, several assumptions are necessary. First, the delay time is minimized when hysteresis threshold region is the narrowest. Second, thermal noise is the main contributor to noise and achieving hysteresis threshold of three times the RMS value of the noise could guarantee a favorable performance for the zero-crossing detection. Third, the power-scaling strategy will yield a speed advantage described below in preamplifiers section.

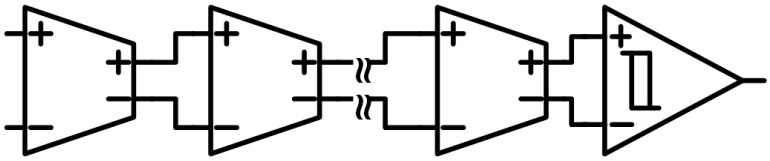


Figure 3.4: Detecting circuits

3.5.1 Preamplifiers

The topology for the single-stage preamplifier is shown in figure 3.5. A fully-differential structure is chosen to achieve high speed. The gain of this structure is determined by the value of $g_m R$. Since the preamplifiers are multi-stage, meaning that they are cascading one after another, the bandwidth of each stage is determined by the load resistances and load capacitances (the following-stage input capacitance).

The optimization strategy used for the preamplifiers is base on power scaling. The power consumption for each stage is scaled down so that the g_m for each stage drops by scaling factor k_s. In addition, the pole for each stage has the same location, and the gain for each stage is designed to be identical; in other words, the gain-bandwidth products are identical. Consequently, the overall small-signal transfer function of the preamplifiers are given by

$$H(s) = \frac{{A_o}^N}{(1 + \frac{s}{\omega_{-3dB}})^N} \tag{3.18}$$

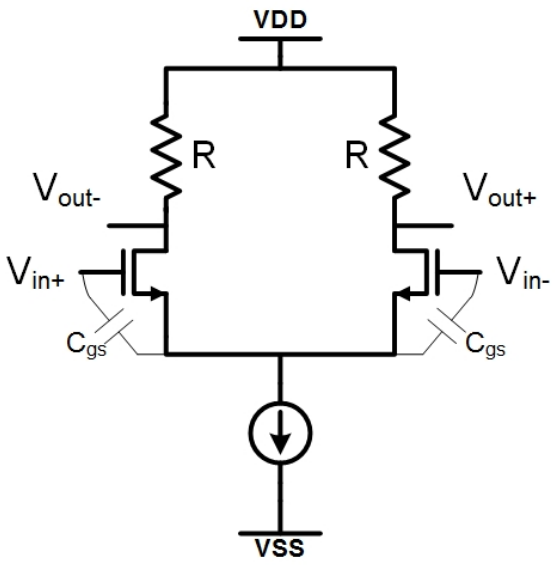


Figure 3.5: Single stage preamplifier

$$g_{m1} = k_s g_{m2} = {k_s}^2 g_{m3} = {k_s}^{N-1} g_{mN} = {k_s}^{N-1} g_m \tag{3.19}$$

Where A_o and ω_{-3dB} is the gain and bandwidth for each stage, respectively and g_m represents the final-stage transconductance value.

$$C_{gs2} = k_s C_{gs3} = {k_s}^2 C_{gs4} = {k_s}^{N-1} C_{gsL} = {k_s}^{N-1} C_{gs} \tag{3.20}$$

Where C_{gs} represents the load capacitor as well as input capacitance of the hysteresis comparator.

The input detection signal behaves like a sinusoid waveform and is used to represent the ringing effect, so the sinusoid static state response can be written as

$$V_{out} = -A_{in} {A_o}^N cos[\omega_{osc} t - N tan^{-1}(\frac{\omega_{osc}}{\omega_{-3dB}})] \tag{3.21}$$

Where A_{in} is the input signal amplitude and ω_{osc} is the oscillation frequency that can be predicted by the unity-gain frequency of the op amp.

There are three principal noise sources shown in Figure 3.6: sampling noise, preamplifier noise and core amplifier noise. The sampling noise is related to the size of the sampling capacitor and is negligible if the sampling capacitor is large. The noise from the core amplifier depends mainly on its input transistor.

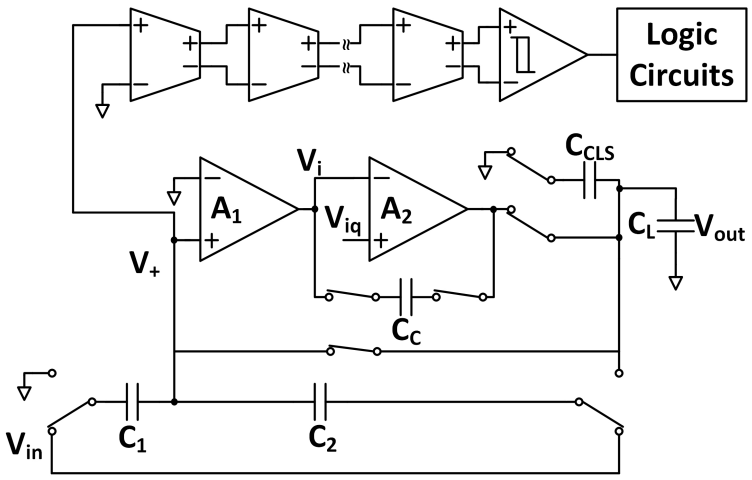


Figure 3.6: SCT overview schematic

The preamplifier's output noise can be calculated by

$$V_{n,rms}{}^2 = \int_0^\infty (\frac{8kT\gamma}{g_{mc}} + \frac{8kT\gamma}{g_{m1}} + \frac{8kT\gamma}{g_{m2}}\frac{1}{A_o} + ... + \frac{8kT\gamma}{g_{mN}}\frac{1}{\prod_{i=1}^{N-1} A_o{}^2})\frac{\prod_{i=1}^{N} A_i{}^2}{[1+(2\pi R_i C_{gs(i+1)} f)^2]^N} df \tag{3.22}$$

Where k is the Boltzmann constant, T is the temperature in degrees Kelvin, γ is the noise coefficient of the transistor, and g_{mc} is the core amplifier's first stage g_m.

3.22 can be simplified into

$$V_{n,rms}{}^2 = [\frac{4kT\gamma}{\pi C_L}(\frac{A_o}{k_s{}^{N-1}}\frac{k_s{}^N - A_o{}^{2N}}{k_s - A_o{}^2}) + \frac{8kT\gamma}{g_{mc}}]f(N) \tag{3.23}$$

where $f(N) = \int_0^\infty \frac{1}{(1+x^2)^N} dx$

We want to set the hysteresis threshold to be three times the RMS value of the noise, so the equation can be written as

$$3V_{n,rms} = -A_{in}A_o{}^N cos[\omega_{osc}t - Ntan^{-1}(\frac{\omega_{osc}}{\omega_{-3dB}})] = 4\sqrt{[\frac{4kT\gamma}{\pi C_L}(\frac{A_o}{k_s{}^{N-1}}\frac{k_s{}^N - A_o{}^{2N}}{k_s - A_o{}^2}) + \frac{8kT\gamma}{g_{mc}}]f(N)} \tag{3.24}$$

$$\omega_{osc}t_{delay} = cos^{-1}[\frac{3}{-A_{in}A_o{}^N}\sqrt{[\frac{4kT\gamma}{\pi C_L}(\frac{A_o}{k_s{}^{N-1}}\frac{k_s{}^N - A_o{}^{2N}}{k_s - A_o{}^2}) + + \frac{8kT\gamma}{g_{mc}}]f(N)} + Ntan^{-1}\frac{\omega_{osc}}{\omega_{-3dB}}] - \frac{\pi}{2} \tag{3.25}$$

The maximum GBW of a single-stage amplifier is given by

$$GB = \frac{g_m}{C_L} = \frac{k_s g_m}{C_g s} = k_s\omega_T = A_o\omega_{-3dB} \tag{3.26}$$

From 3.26 we obtain

$$\frac{\omega_{osc}}{\omega_{-3dB}} = \frac{A_o \omega_{osc}}{k_s \omega_T} \tag{3.27}$$

An design example will be provided using $\frac{\omega_{osc}}{\omega_T} = \frac{20M}{4G}$, $A_o = 5$ and $C_L = 10fF$. The numerical simulation result were obtained using Matlab are shown in Figure 3.7.

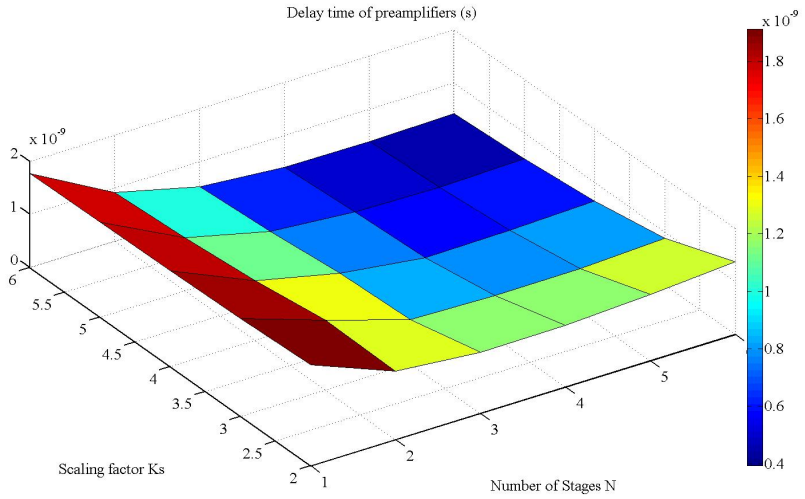


Figure 3.7: Normalized delay time vs. scaling factor and number of stages

From Figure 3.7, we can determine that the delay time is huge for a single-stage preamplifier and then gradually decreases as the number of stages increases. The power-scaling factor also improves the preamplifier response. However, further increasing the number of stages and scaling factor would not help reduce the delay time.

3.5.2 Hysteresis comparator

The schematic for the hysteresis comparator [14] is shown in Figure 3.8 below that has a fully-differential input and single-ended output topology. M_1 and M_2 are input differential pairs. M_3 and M_4 form cross-coupled pairs that provide positive feedback and M_5 and M_6 are load transistors. M_7-M_{10} operate as current mirrors and provide a class AB output stage. The hysteresis performance is accomplished by the internal positive feedback loop. So long as the ratio $\frac{S3}{S5}$ is smaller than one, there is no transfer-curve hysteresis. When the ratio is large than one, there will be a hysteresis effect.

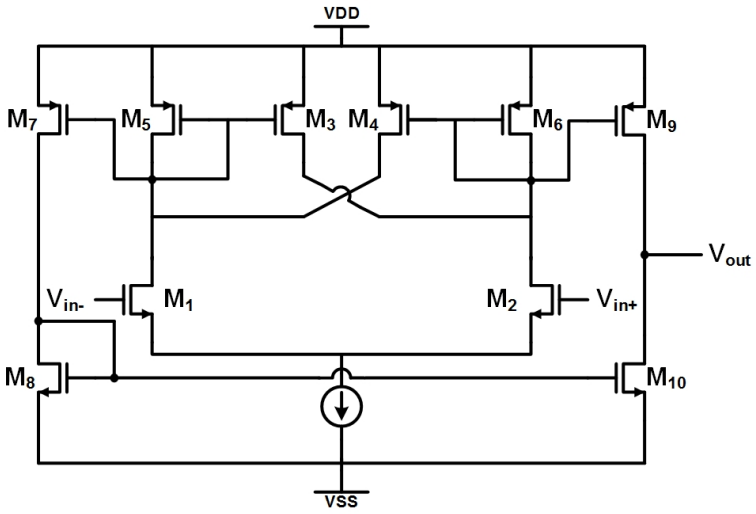


Figure 3.8: Schematic of hysteresis comparator

Assume that the inverting input of the hysteresis comparator is tied to ground while the non-inverting input is set at a value much less than zero, so M_1 is on and M_2 is off. All the tail current will flow into M_1, but M_3 and M_5 do not behave like a current mirror. When the input voltage of non-inverting input is rising, M_2 begins to conduct. When the gate voltage of the non-inverting input reaches a value at which the current is equal to the current consumed in M_1 times the current mirror ratio, positive feedback will "force" the output signal polarity to change instantaneously. The current-mirror ratio and the tail current are M and I_{tail}, respectively. The tripping point can thus be expressed as:

$$V_{TRP}^{+} = \sqrt{\frac{2MI_{tail}}{(M+1)S_2}} + V_{T2} - \sqrt{\frac{2I_{tail}}{(M+1)S_1}} + V_{T1} \tag{3.28}$$

On the other hand, the tripping point of the hysteresis comparator is the same value but with opposite sign.

3.5.3 Logic circuits

The detection circuits require digital logic to control the switches for SCT operation. A schematic diagram is shown in Figure 3.9. The input to the logic circuits come from the inverting input of the core amplifier (V_+ in Figure 3.1). The logic circuits have four output signals: CLK_ls, CLK_lsb, CLK_c and CLK_cb. Signal VSET is generated by a comparator

during the sampling phase in order to determined whether or not the input signal is positive. Signals $CLK1$, CLK1_b, $CLK2$ and CLK2_b are generated by the clock generator; they are non-overlapping complementary clocks. $CLK1$ and CLK1_b are complementary clocks for the sampling phase while $CLK2$ and CLK2_b are complementary clocks for the amplification phase (in the SCT, they contain a rapid estimation phase, a level-shifting phase and a critically-damped phase). Detailed information about these four clocks will be given in the following clock generator section.

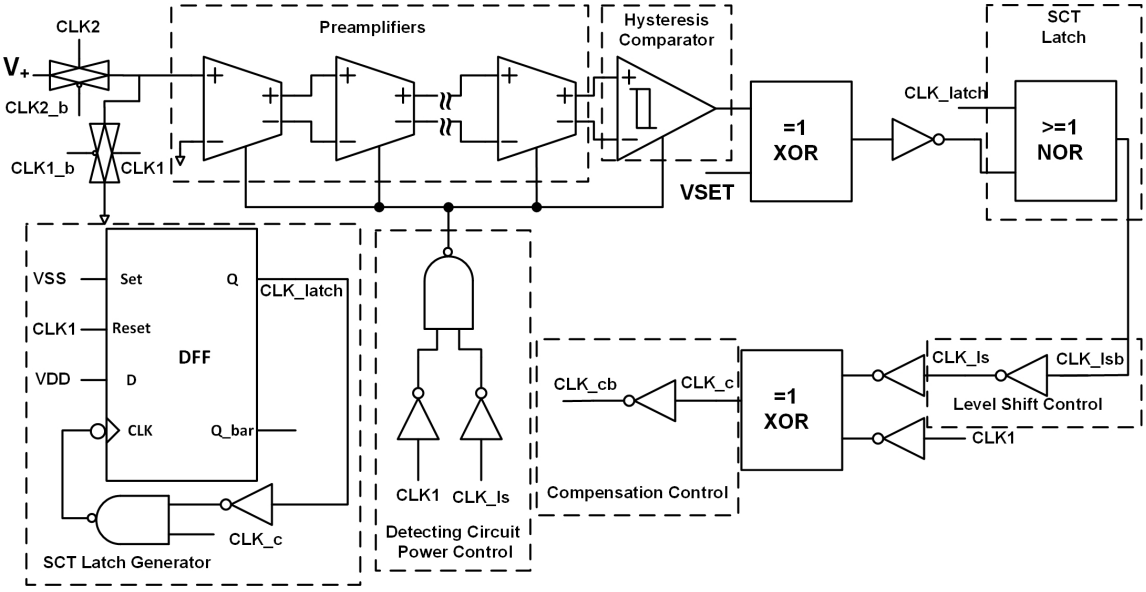


Figure 3.9: Digital logic circuits

Complementary signal CLK_ls and CLK_lsb control the level-shifting operation, while complementary signal CLK_c and CLK_cb determine the critically-damped phase timing. From 3.9, we know that the level- shifting phase clock signal occurs earlier than the critically-damped phase signal. Since the compensation control signal is operating during both sampling phase and critically-damped phase, CLK1 signal is also needed following CLK_ls to create CLK_c and CLK_cb.

The detection circuit power control block guarantees that the preamplifiers and hysteresis comparators are only operating at rapid estimation phase so that their overall power consumption can be minimized. An SCT latch circuit is also required. Because digital logic only needs to be triggered once each cycle, we want the digital logic circuit to remain in latch after the

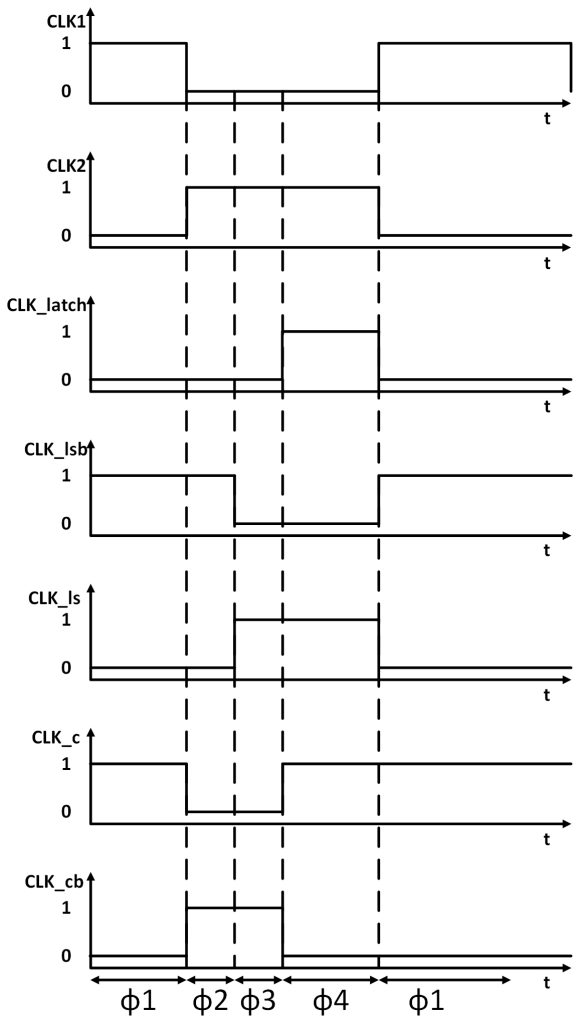


Figure 3.10: Timing for Digital logic circuits

critically-damped phase until the next sampling period starts. This can be achieved by using SCT latch generator built from a negative edge-triggered D flip-flops and other combination logic circuits. Detailed schematics for D flip-flops and combinational logic are provided in Appendix.

The timing diagram for the digital logic circuits is shown in Figure 3.10 where $\phi 1$, $\phi 2$, $\phi 3$, $\phi 4$ represent sampling, rapid estimation, level-shifting and critically-damped phase, respectively.

3.6 Clock generator

The flip-around switched-capacitor amplifier requires several clock signals to control the conventional sampling and amplification phases, including complementary non-overlapping clock signals $CLK1$, CLK1_b, $CLK2$ and CLK2_b. Moreover, complementary clocks signal CLK1p and CLK1−p_b prior to $CLK1$ are also required to control the timing of the buffer-connected switches in order to minimize the charge-injection issue. The SCT schematic diagram showing these switches is given in Figure 3.11. All switches are built using transmission gates. Clock signals CLK_ls, CLK_lsb, CLK_c and CLK_cb were discussed in the previous chapter. CLK_ls_d, CLK_lsb_d are generated from CLK_ls and CLK_lsb by adding delay.

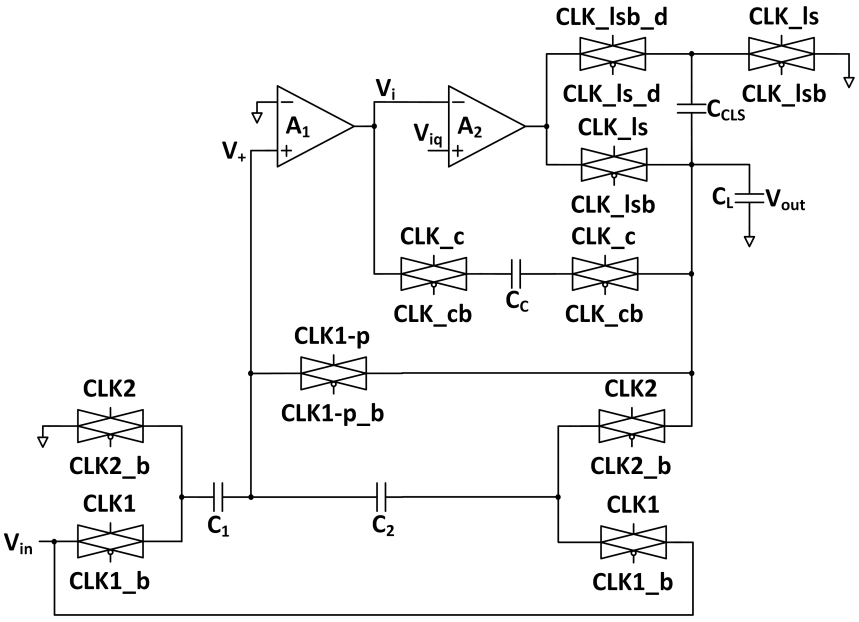


Figure 3.11: SCT schematic with switches

The clock generator is used to generate the complementary non-overlapping clock signals $CLK1$, CLK1_b, CLK1−p, CLK1−p_b, $CLK2$, $CLK2$ and CLK2_b. The overall diagram of these signals is given in Figure 3.12. There are two main parts: the non-overlapping clock generator and the complementary clock generator. The non-overlapping clock generator creates two non-overlapping clocks that are fed into complementary clock generator so that each non-overlapping clock will create a pair of complementary clocks.

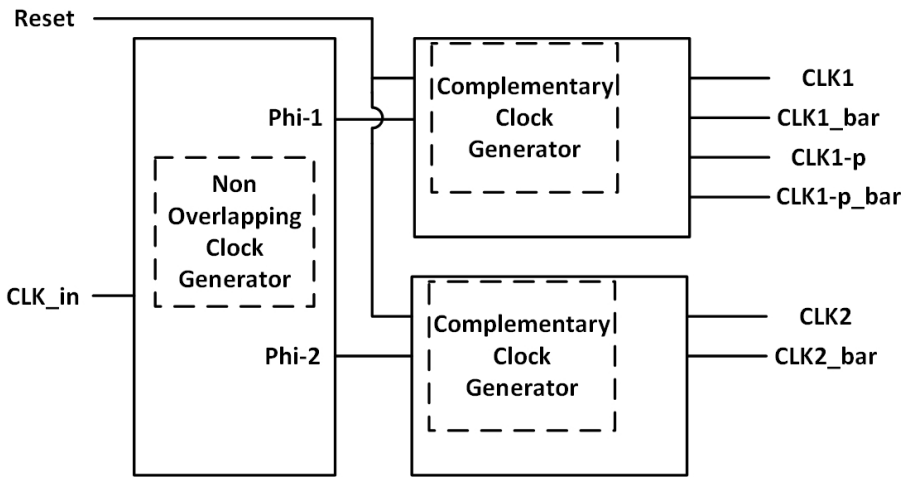


Figure 3.12: Overview of clock generator

In Figure 3.13, external clock CLK_in is the input to the non-overlapping clock generator and $Phi-1$ and $Phi-2$ are the outputs. The non-overlapping period can be controlled by inverter and NOR gate delays.

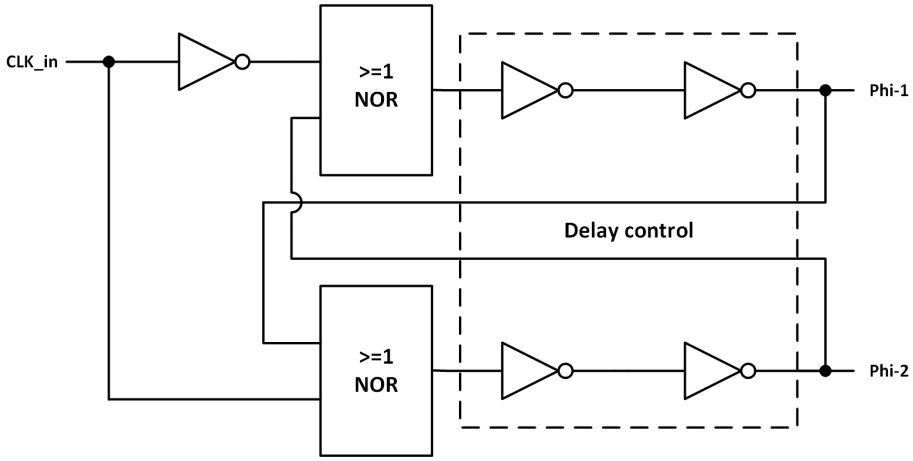


Figure 3.13: Non-overlapping clock generator

Figure 3.14 shows the schematics diagrams for the complementary clock generator. A double-edge-triggered D flip-flops (DE−DFF) is used to generate complementary clock signals for each non-overlapping clock. A chain of inverters act as driving stages needed because of the large loading capacitor (several switches in Figure 3.11). A detailed schematic diagram for the double-edge-triggered D flip-flops is given in the Appendix.

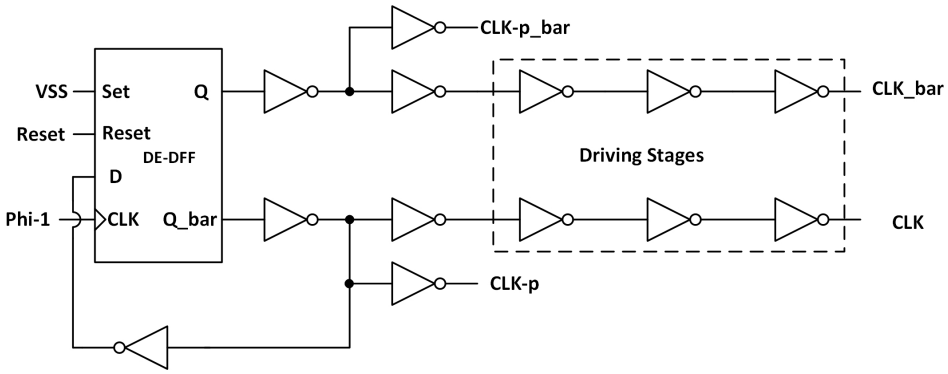


Figure 3.14: Complementary clock generator

The timing diagram for the non-overlapping complementary clock is shown in Figure 3.15 in which both the rising edge and falling edge are shown. $\phi 1$ and $\phi 2$ represent sampling and amplification phase respectively.

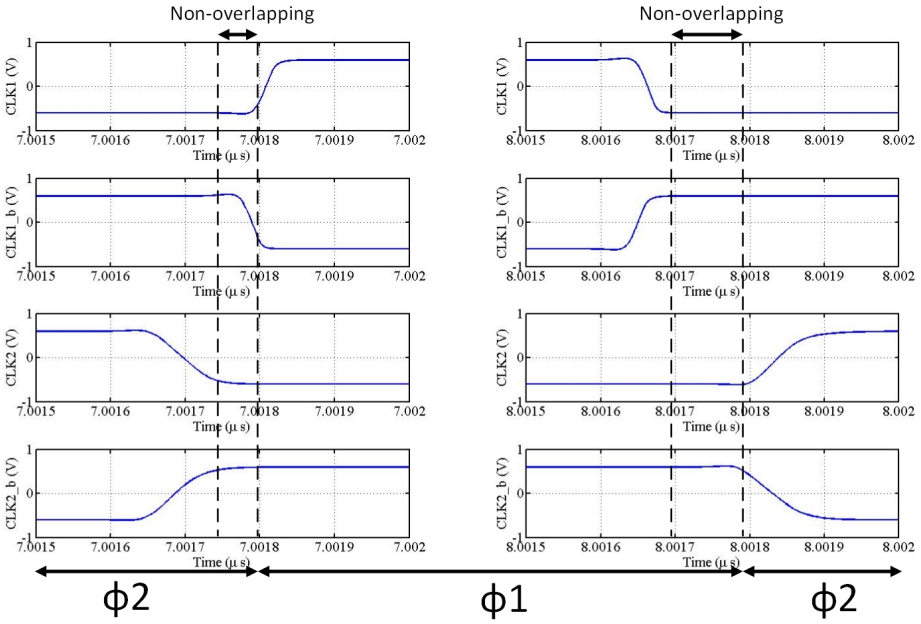


Figure 3.15: Timing diagram for non-overlapping complementary clock

The transient waveform of each node with SCT is shown in Figure 3.16 for an input signal amplitude is 20 mV. Four major control signals CLK1, CLK2, CLK_ls and CLK_c are shown. CLK1 and CLK2 are generated by the non-overlapping complementary clock generator while CLK_ls and CLK_c are generated by the detection circuits.

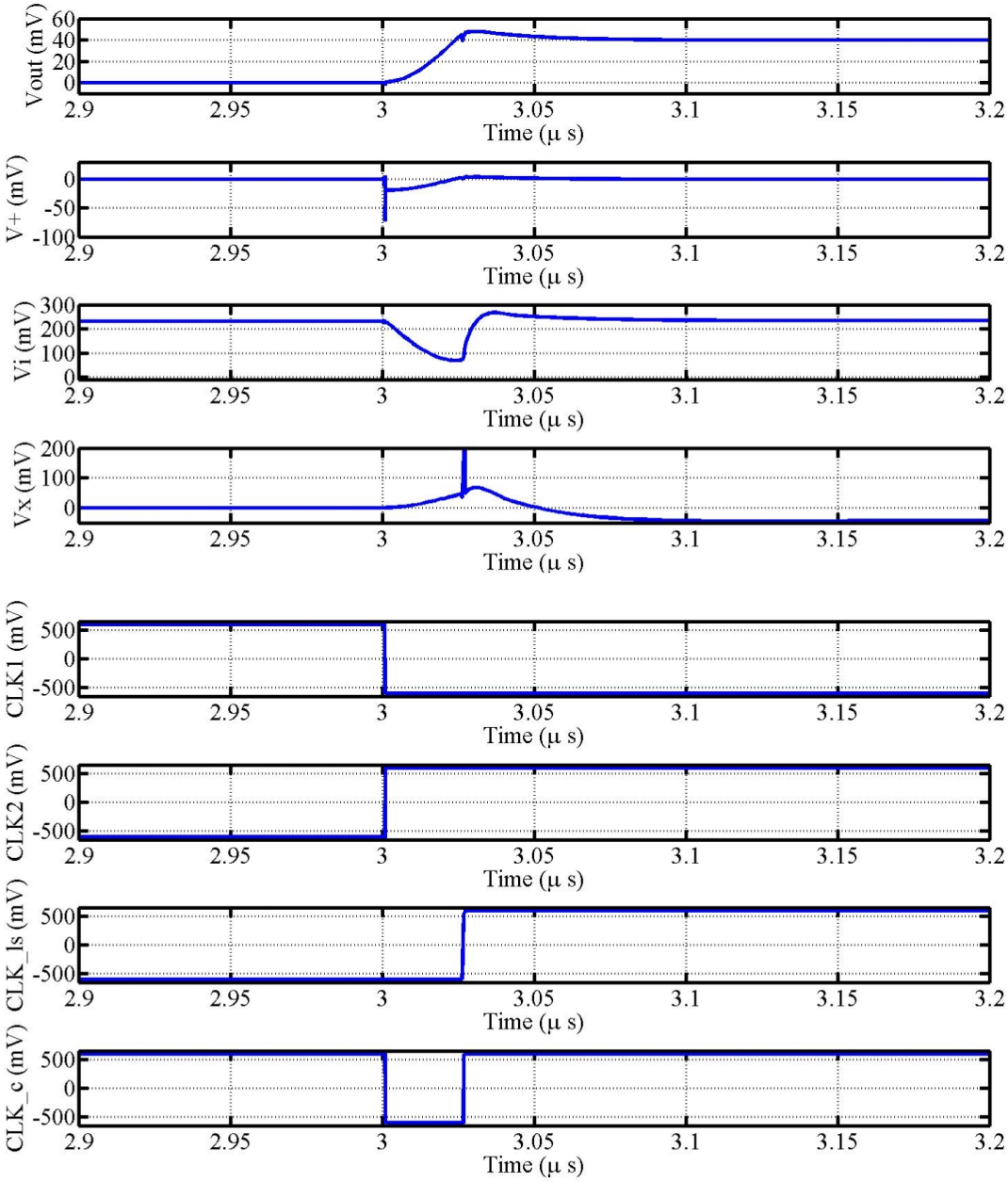


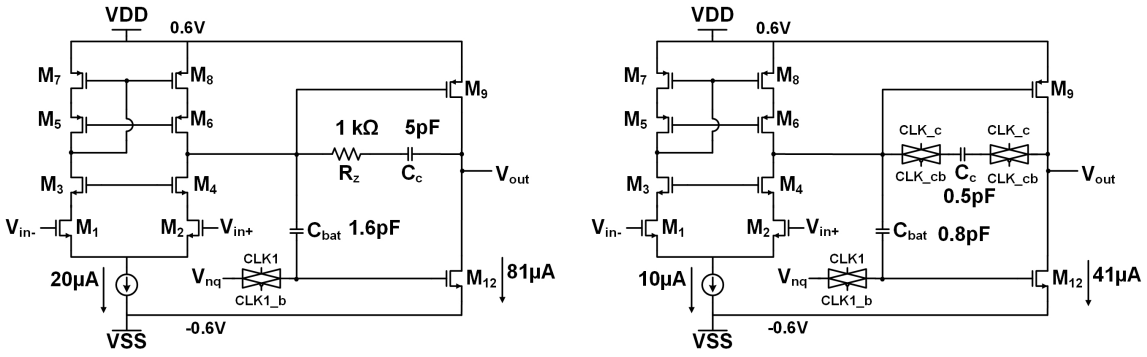
Figure 3.16: Transient signal and clock waveform

CHAPTER 4. SCT IMPLEMENTATION AND SIMULATION RESULTS

To validate SCT, two switched-capacitor amplifiers for multiplying digital-to-analog converter (MDAC) application were designed using a 0.13μm CMOS process. Both had telescopic input stages with Miller compensation and nulling resistors. The first stage is cascode while the second stage had a Class AB output so that both charging and discharging process can be accelerated. The supply voltages are set to be $\pm$ 0.6V.

4.1 SCT implementation

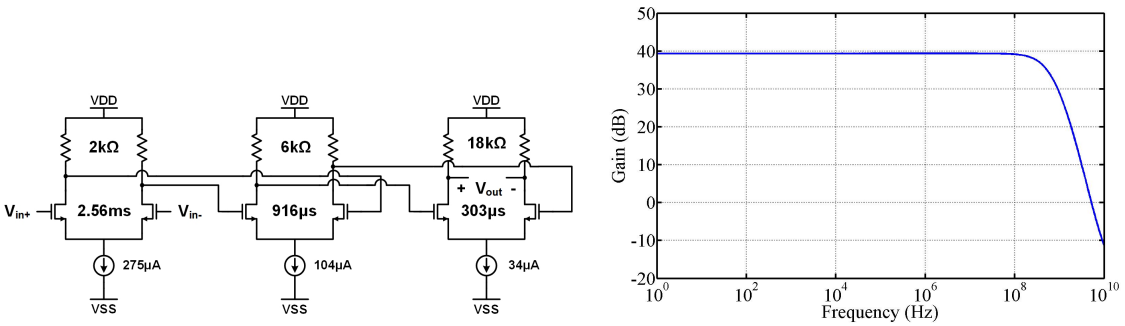
The schematic diagrams for the core amplifier are shown in Figure 4.1. They are two stage amplifiers with telescopic cascode input stages and class AB output stages. Miller compensation with nulling resistors is used for compensation. To reduce detection-circuit requirements, the SC amplifier with SCT was designed for low quiescent power consumption compared to the conventional case. For the SC amplifier with SCT, switches were connected to the compensation capacitor to make it perform like a nulling resistor. This class AB structure was built using an AC coupling capacitor C_{bat}[32]. The battery capacitor is designed to be ten times larger than the parasitic capacitance at the gate of $M12$ to achieve satisfactory class AB output. The current consumption for the conventional core amplifier is 20μA and 81μA for the first stage and second stage, respectively. The current consumption for the SC amplifier with SCT is only 10μA and 41μA for the first and second stage, respectively. The load capacitor (C_L) and feedback capacitors (C_1,C_2) are all 40 pF. The compensation capacitor is only 500 fF compared to the conventional 5 pF. The nulling resistor used in the conventional SC amplifier is 1 $k\Omega$ and the CLS capacitor is 5 pF. The battery capacitor C_{bat} is 1.6 pF and 0.8 pF for the conventional SC amplifier and the SC amplifier with SCT, respectively.



(a) (b)

Figure 4.1: Core amplifier (a)conventional,(b)SCT

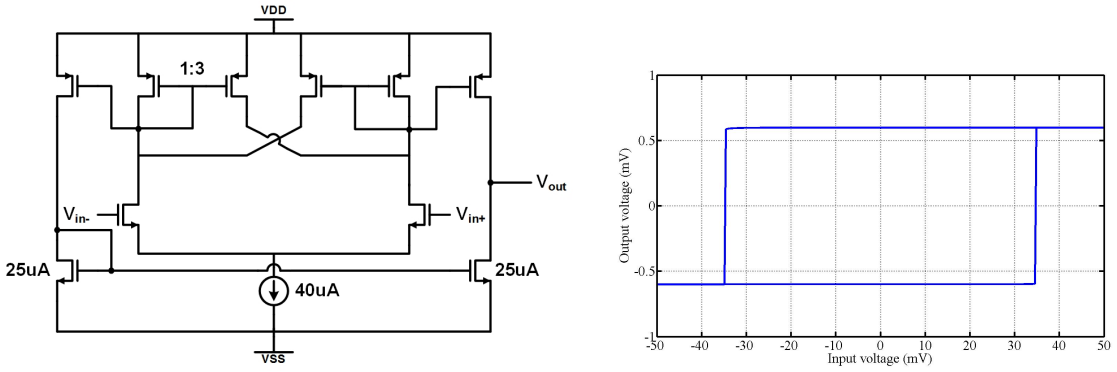
A four stage preamplifier provides a portion of the detection circuitry. A schematic diagram of the preamplifier is give in Figure 4.2(a). The design strategy is based on power scaling. The number of stages is three and the power (g_m) scaling factor is three as well. The frequency response of the preamplifier is shown in figure 4.2(b). The gain of the preamplifiers are 39 dB and the bandwidth is 418 MHz for a 10 fF load.



(a) (b)

Figure 4.2: Preamplifier (a)Schematic of preamplifiers,(b) Frequency response of preamplifiers

Based on the noise analysis given in Chapter 3, the $V_{n,rms}$ can be calculated to be 10 mV, so the hysteresis threshold was chosen to be three times the $V_{n,rms}$, i.e., 30 mV. The current arrangement for the hysteresis comparator is shown in Figure 4.3(a) and the current mirror ratio M was chosen to be three. The DC sweep simulation is given in Figure 4.3(b). The upper and lower thresholds for the hysteresis comparator are ±36 mV.



(a) (b)

Figure 4.3: Hysteresis comparator (a)Schematic of hysteresis comparator (b) DC sweep of hysteresis comparator

4.2 Simulation results

The effective performance of the SCT will be compared to that of a conventional SC circuit. Since the two switched-capacitor amplifiers have class AB output stages, both positive and negative input signals will be considered. The transient simulation results for several input signals are shown in Figure 4.4 in which the blue curve represents the SC amplifier with SCT and the red curve represents a conventional SC amplifier. It is clear that the blue curve settles much faster that the red one.

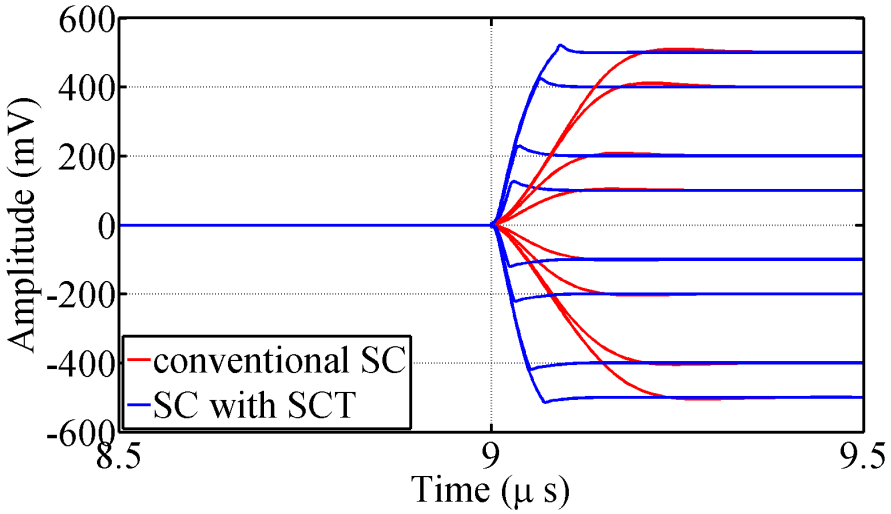
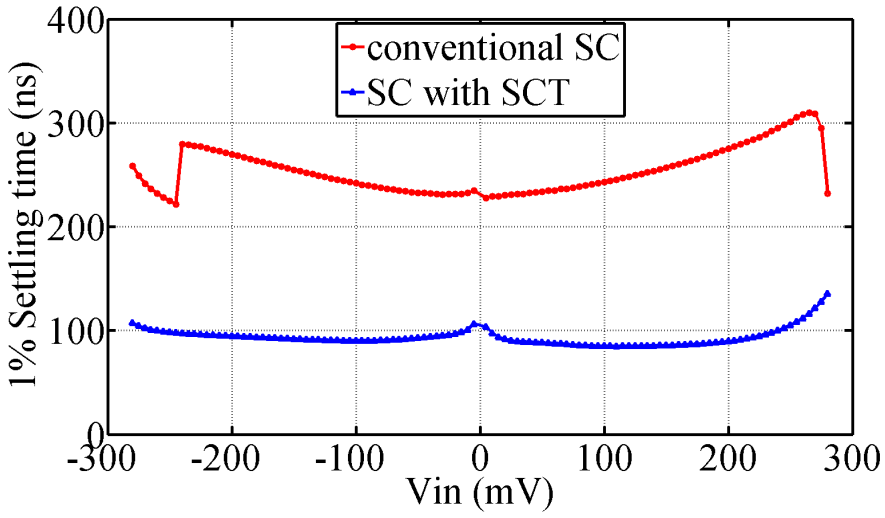
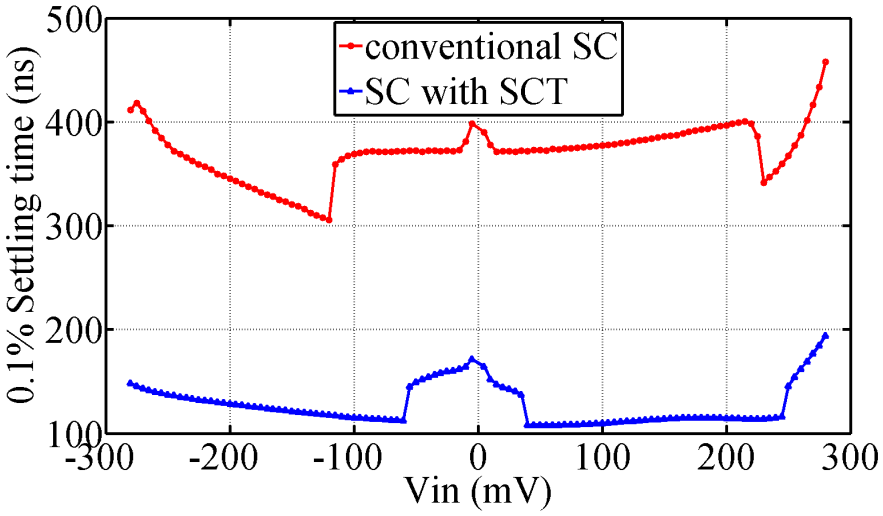


Figure 4.4: Transient simulation SC amplifier

The 1% and 0.1 % accuracy settling times of both two op amps for different input signal amplitudes is shown in Figure 4.5(a) and Figure 4.5(b). It can be seen that these settling times are reduced by more than 60% on average.



(a)



(b)

Figure 4.5: Settling time (a)1% error settling accuracy (b) 0.1% error settling accuracy

The percentage overshoot for different input signal amplitudes is shown in Figure 4.6. For small input signal amplitudes, the SC amplifier with SCT exhibit larger overshoot due to the slower response of its detection circuit, but this does not affect the settling time. In addition,

neither of these two SC amplifiers could support rail-to-rail performance because of reduced gain. Thus, the input signal amplitude was simulated for the range -280 mV to 280 mV for 1% and 0.1% accuracy settling.

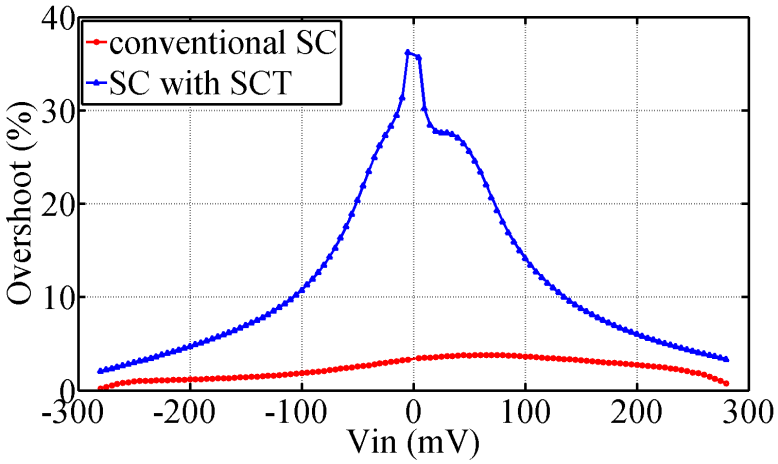


Figure 4.6: Overshoot in percentage

The overall dynamic power was also simulated for a 1 MHz clock signal and a 150 mV input signal amplitude. The overall transient current consumption for one period is shown in Figure 4.7 in which the blue curve represents the SC amplifier with SCT and the red curve represents the conventional SC amplifier. The overall transient current consumption is low except during the rapid estimation phase when the detection circuits are operating.

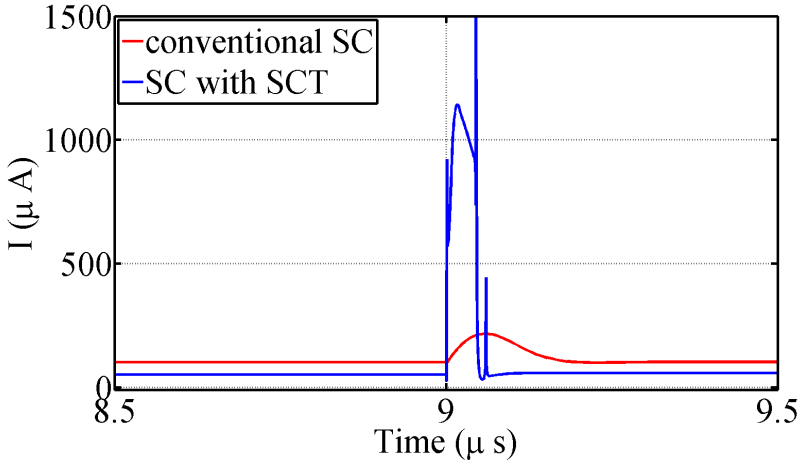


Figure 4.7: Overall transient current consumption

Each period average current consumption for different input signal amplitude is shown in Figure 4.8. Revealing that the average current consumption for most input signal amplitude is less when using SCT.

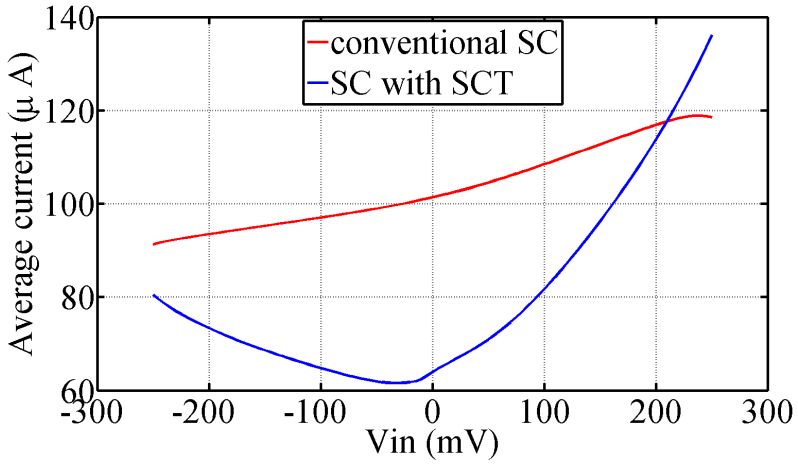


Figure 4.8: Average current consumption

The overall performance is summarized in Table 4.1. Most parameters benefit a great deal by using SCT. The only drawback for SCT is that there is an area overhead of about 10% due to the area consumed by the detection circuits.

Table 4.1: Performance summary of the switched-capacitor amplifier

Parameter	**Conventional**	**SCT**
DC gain (dB)	80	80
C_{Load},$C_{feedback}$ (pF)	40	40
1% $t_{settling}$ (μs)	254	94
0.1% $t_{settling}$ (μs)	371	128
C_C (pF)	5	0.5
C_{CLS} (pF)	N/A	5
I_Q (μA)	101	51
Total average power (μW/μs)	124	96
Estimated area (μm^2)	4009	4525
Supply voltage (V)	$\pm$ 0.6	$\pm$ 0.6
Technology (nm)	130	130

CHAPTER 5. CONCLUSION AND FUTURE WORK

5.1 Summary

In this thesis, a switched-compensation technique (SCT) is proposed as a novel discrete-time based compensation method for use in switched-capacitor circuits. By using SCT, the settling time and quiescent power consumption can be reduced. SCT operation including detection circuits was investigated. As an example, SCT was implemented into a flip-around switched-capacitor amplifier. To achieve fast settling performance, a poorly (or even not) compensated core amplifier is required. Because of its large unity gain frequency, the overall SC amplifier can respond rapidly during the beginning of its amplification phase. The improved performance is achieved by taking advantage of the initially under-damped ($\xi \ll 1$) transient response and then converting the system into a critically-damped configuration ($\xi \approx 1$) without affecting the output waveform. Even though a small signal settling process is still required due to the delay time induced by the detection circuits (which indeed causes overshoot), a faster settling performance can still be achieved. The overshoot is large when the signal amplitude is small but this does not affect the overall settling performance. Mathematical derivation and transistor level circuit simulation validate the advanced properties and improved performance of the proposed SCT. Compared to the conventional flip-around SC amplifier, 1% and 0.1 % accuracy settling times are reduced by more than 60% on average while consuming only half the amount of quiescent power. In addition, the overall average power consumption is reduced by 20%. Several design considerations, including the SC amplifier, the clock generator and detection circuits, are also discussed in this thesis. The technique described is suitable for switched-capacitor applications where fast settling performance and low static power dissipation is required.

For future work, more effort will be expanded in modifying the current version into a fully-differential structure. Because of power scaling, achieving satisfactory signal to noise ratio is becoming an increasingly critical problem. Since a fully-differential structure could double the signal to noise ratio, more and more MDACs used in the pipeline ADC are accepting this structure. Optimization strategies for power conservation in detection circuits to minimize delay time could be further investigated. Moreover, pipeline ADCs could be built using SCT to examine pros and cons from the system level.

APPENDIX A. ADDITIONAL MATERIAL

In this chapter, several digital logic circuits provided in the previous chapters will be given in detail.

the NOR gate utilized in non-overlapping clock generator is shown in Figure A.1.

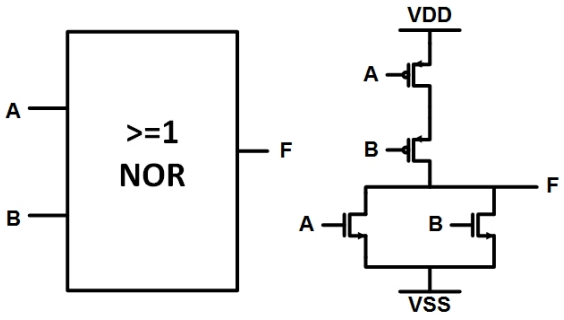


Figure A.1: NOR gate

the XOR gate used in logic circuits is shown in Figure A.2.

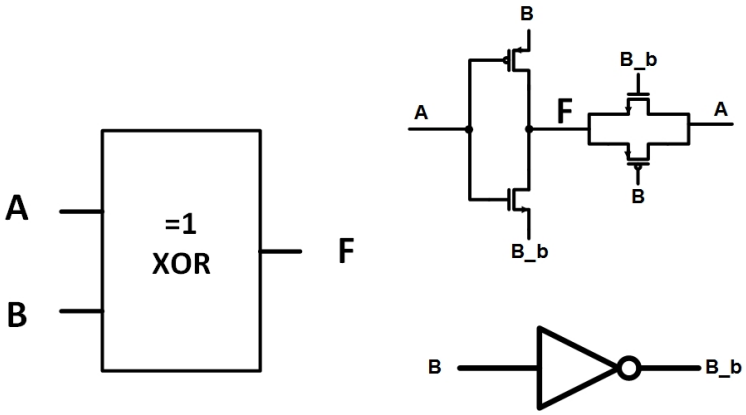


Figure A.2: XOR gate

the D flip-flops used in both logic circuits and clock generator is shown in Figure A.3. Here we should mention that the D flip-flops given is a positive edge triggered D flip-flops. The neg-

ative edge triggered D flip-flops can be easily obtained by removing the first inverter connect with the CLK input.

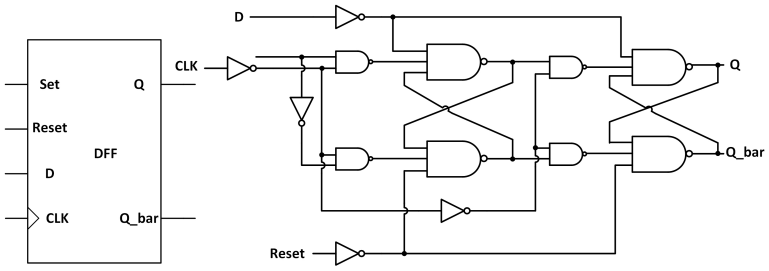


Figure A.3: D flip-flops

The Mux used in double edge triggered D flip-flops is shown in Figure A.4.

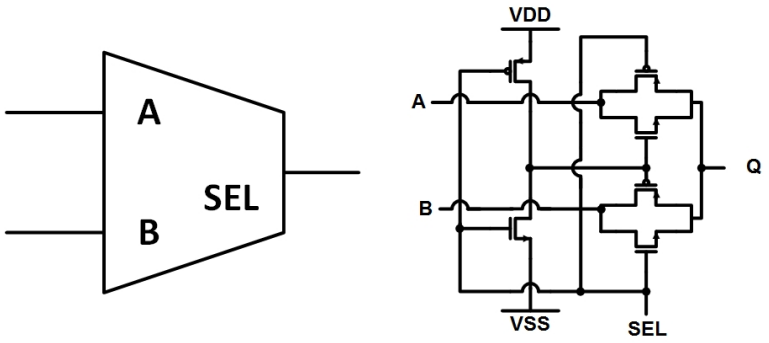


Figure A.4: Mux

The double edge triggered D flip-flops used in complementary clock generator is shown in Figure A.5. Both positive edge triggered and negative edge triggered D flip-flops are needed.

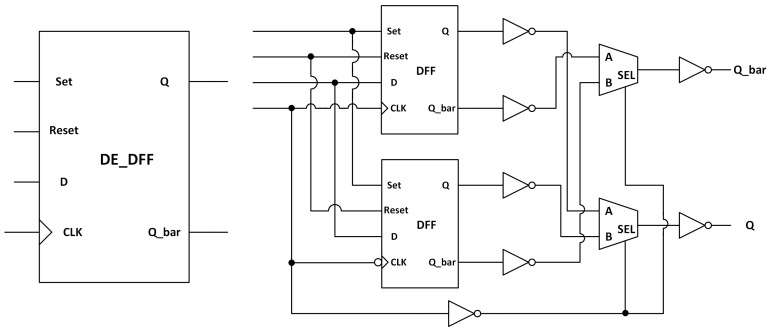


Figure A.5: Double edge triggered D flip-flops

BIBLIOGRAPHY

[1] A. Danowitz, K. kelley, J. Mao, JP. Stevenson, and M. Horowitz, "CPU DB: Recording Microprocessor History, "Communication of the ACM, vol. 55, no.4, Apr. 2012.

[2] K. N. Leung and P. K. T. Mok, "Analysis of multistage amplifier-frequency compensation, "IEEE Trans. Circuits Syst. I, Fundam. Theory Appl., vol. 48, no. 9, pp.1041-1056, Sep. 2001.

[3] F. You, S. H. K. Embabi, and E. Sanchez-Sinencio, "Multistage amplifier topologies with nested Gm-C compensation, "IEEE J. Solid-State Circuits, vol. 32, pp.2000-2011, Dec. 1997.

[4] R. G. H. Eschauzier, L. P. T. Kerklaan, and J. H. Huijsing, "A 100 MHz 100 dB operational amplifier with multipath nested miller compensation structure, "IEEE J. Solid-State Circuits, vol. 27, pp.1709-1717, Dec. 1992.

[5] H. T. Ng, R. M. Ziazadeh, and D. J. Allstot, "A mulitstage amplifier technique with embedded frequency compensation, "IEEE J. Solid-State Circuits, vol. 34, pp.339341, Mar. 1999.

[6] K. N. Leung, P. K. T. Mok, W. H. Ki, and J. K. O. Sin, "Damping-factor-control frequency compensation technique for low-voltage low-power large capacitive load applications, "in Dig.Tech. Papers ISSCC99, 1999, pp.158159.

[7] K. N. Leung, P. K. T. Mok, W. H. Ki, and J. K. O. Sin, "Three-stage large capacitive load amplifier with damping-factor control frequency compensation, "IEEE J. Solid-State Circuits, vol. 35, pp.221230, Feb. 2000.

[8] B. Ahuja, "An improved frequency compensation technique for CMOS operational amplifiers,"IEEE J. Solid-State Circuits, vol. SC-18, pp.629633, Dec. 1983.

[9] B. Huang, Degang Chen, "Advancements on Crossbar-Based Nanoscale Reconfigurable Computing Platforms, "Proc. 57rd IEEE International Midwest Symposium on Circuits and Systems(MWSCAS), pp.270-273, USA, Aug 2014.

[10] B.W. Lee, and B.J Sheu, "A high slew-rate CMOS amplifier for analog signal processing, "IEEE J. Solid-State Circuits, vol.25, no.3, pp.885-889, June 1990.

[11] M. Degranuwe, J. Rijmenants, E. A. Vittoz, and D. Man, "Adaptive biasing CMOS amplifiers, "IEEE J. Solid-State Circuits, vol.17, no.3, pp.522-528, June 1982.

[12] A.J. Lopez-Martin, S. Baswa, J. Ramirez-Angulo, and R.G. Carvajal, "Low-Voltage Super class AB CMOS OTA cells with very high slew rate and power efficiency, "IEEE J. Solid-State Circuits, vol.40, no.5, pp.1068-1077, May 2005.

[13] B. Razavi, "Design of analog CMOS integrated circuits, "Boston, McGraw-Hill, 2001.

[14] P. E. Allen, D R. Holberg, "CMOS Analog Circuit Design, "2nd edition, New York, Oxford, 2002.

[15] M. Yavari and O. Shoaei, "Low-voltage low-power fast-settling CMOS operational transcondutance amplifiers for switched-capacitor applications, "IEE Proc. Cir., Dev. Sys, pp. 573-578, Dec. 2004.

[16] K. Bult and G. J.G . M. Geelen, "A fast-setting CMOS op amp for SC circuit with 90-dB DC gain, "IEEE J. Solid-State Circuits, vol. 25, pp. 1379-1384, Dec. 1990.

[17] H. Yang and D. Allstot, "Considerations for fast settling operational amplifiers, "IEEE Trans. Circuits Syst, vol. 37, no. 3, pp. 326334, Mar. 1990.

[18] R. Castello and P. R. Gray, "A High-performance micropower switched-capacitor filter, "IEEE J. Solid-State Circuits, vol. 20, no. 6, pp. 1122-1128, Dec. 1985.

[19] M. G. Degrauwe, J. Rijmenants, E. A. Vittoz, and J. J. D. Man, "Adaptive biasing CMOS amplifiers, "IEEE J. Solid-State Circuits, vol. SC-17, no. 6, pp. 522528, Jun. 1982.

[20] B. R. Gregoire and U. K. Moon, "An over 60-dB true rail-to-rail performance using correlated level shifting and an op-amp with 30-dB loop gain, "IEEE J. Solid-State Circuits, vol. 43, no. 12, pp. 2620-2630, Dec. 2008.

[21] R. Gregorian, K. Martin and G. Temes "Switched capacitor circuit design, "Proceeding of the IEEE, Vol. 71, No. 8, pp. 941-966, 1983.

[22] G.Jacobs, D. Allstot, R.Brodersen, P. Grey "Design Technique for MOS switched Capacitor Ladder Filters, "IEEE Trans. Cir. and Syst., vol. 25, pp. 1014-1021, Dec. 1978.

[23] Richard Markell, "Take the Mystery Out of the switched-capacitor filter: The system Designer's Filter Compendium, "Linear Technology Application Note 40, 1990.

[24] G. Temes, "Finite Amplifier Gain and Bandwidth Effects in Switched-Capacitor Filters, "IEEE J. Solid-State Circuits, vol. 3, no. 3, pp. 358-361, Jun. 1980.

[25] M. Ghaderi, Josef. Nossek, G. Temes, "Narrow-Band Switched-Capacitor Bandpass Filters, "IEEE Trans. Cir. and Syst., vol. 29, no. 8, pp. 557-572, Aug. 1982.

[26] H. Yoshizawa, "High-linearity switched-capacitor circuits in digital CMOS technologies, "Ph.D. dissertation, Oregon State University, Corvallis, OR, 1997.

[27] H. Yoshizawa, Y. Huang, P. Ferguson, G. Temes, "MOSFET-Only Switched-Capacitor Circuits in Digital CMOS Technology, "IEEE J. Solid-State Circuits, vol. 34, no. 6, pp. 734-747, Jun. 1999.

[28] D. Allstot, R. Brodersen, P. Gray, "MOS Switched Capacitor Ladder Filters, "IEEE J. Solid-State Circuits, vol. 13, no. 6, pp. 806-814, Dec. 1978.

[29] Y. Kamath, R. Meyer, and P. Gray, "Relationship between frequency response and settling time of operational amplifier, "IEEE J. Solid-State Circuits, vol. 9, no. 6, pp. 347352, Dec. 1974.

[30] B. Hosticka, R. Brodersen, P. Grey, “MOS Sampled Data Recursive Filter Using Switched Capacitor Integrators, ”IEEE J. Solid-State Circuits, vol. 12, no. 6, pp. 600608, Dec. 1977.

[31] J. Mitola iii, “Software radios: Survey, critical evaluation and future directions, ”in Proc. Telesyst. Conf., pp11/13-13/23, 1992.

[32] J. Ramrez-Angulo, R. G. Carvajal, J. A. Galn, and A. Lpez-Martn, “A free but efficient low-voltage class-AB two-stage operational amplifier, ”IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 53, no. 7, pp. 568571, Jul. 2006.